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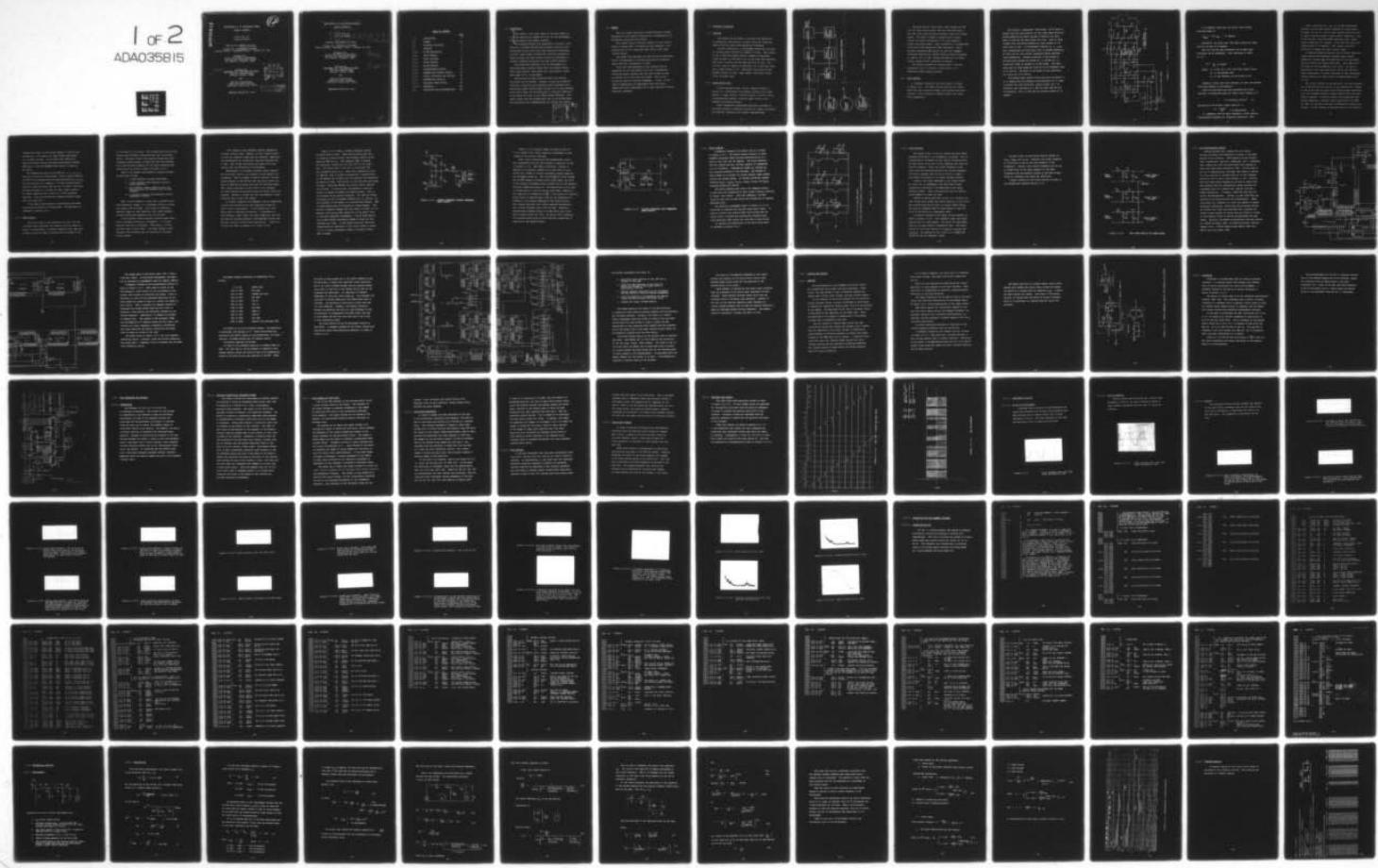
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DEVELOPMENT OF AN INTEGRATED POWER
MODULE INVERTER

(12) B.S.

Final Type III
Technical Report

Contract No. DAAK02-75-C-0101

Project No. A231/~~B24175~~ 5A230350
Contract Dates - September 9 1974 - October 30, 1976

Prepared For
U. S. Army Mobility Equipment
Research and Development Center
Ft. Belvoir, Virginia 22060

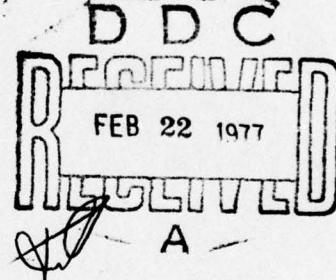
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1.0 INTRODUCTION

This report is the final report of the work effort on U.S. Army Contract No. DAAK02-75-C-0101 for the development of an Integrated Power Module Inverter.

This research project was established to provide a cost effective, reliable and efficient converter using an integrated power switch with pulse width modulation techniques. Low cost, light weight and efficient converter systems are highly suitable and offer weight and quality advantages in portable frequency conversion and power control systems.

This particular program is for the development of a 15KW three phase inverter system which can convert unregulated, poor quality, input power into, good quality, three phase power at 50, 60 and 400Hz.

Much success has been achieved toward the intended objectives and the program. However, it must be recognized that when a radically new technology using techniques which effectively reduce system weight as much as 67%, some problems arise which reduce the available time to allow for completion of all goals set forth in this "best efforts" program. This report states what was accomplished, how it was accomplished, and conclusions and recommendations for further work effort.

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2.0 SUMMARY

This is a report providing a system overview, a detail discussion of the technical approach and recommendation and conclusions concerning this project.

This report gives a technical analysis of the inverter system in enough detail to assess how each component is an integral part of the Integrated Power Switch (IPS) power inverter system.

The report also discusses how the IPS can be controlled using a microprocessor to provide good quality sinusoidal output from raw, unregulated, AC power.

While the final packaging of the inverter and its components has not been made on this unit, calculations concerning weight indicate that the final weight of such an inverter can be less than 100 pounds. This is substantially below all existing equipment. In fact, it provides an approximate 67% improvement over the nearest competition and an improvement of at least 200% over existing commercial equipment.

3.0 TECHNICAL DISCUSSION

3.1 OVERVIEW

The purpose of the effort is to prove the feasibility of generating, good quality, AC power using the integrated power switch and pulse width modulation techniques.

To prove feasibility, a development effort was initiated by the Army under Contract No. DAAK02-75-C-0101. This effort is for a 15KW three phase inverter capable of generating output AC power of 120V RMS at 50, 50 and 400Hz when measured from line to neutral and 208 VRMS from line to line. The inverter must be capable of operating into a load that looks like a power factor of 0.8. Additional objectives of this program include low cost, light weight, efficiency, reliability and small size.

3.2.0 SYSTEM DESCRIPTION

A block diagram of the inverter system is shown in Figure 3.1. Functionally the inverter consists of an input section, a boost circuit, a switch section, a filter section, a microprocessor section, auxiliary power section and a feedback and control section.

Other information highlighted separately and shown on the block diagram as important entities are coding, evaluation and analysis, mechanical and thermal considerations.

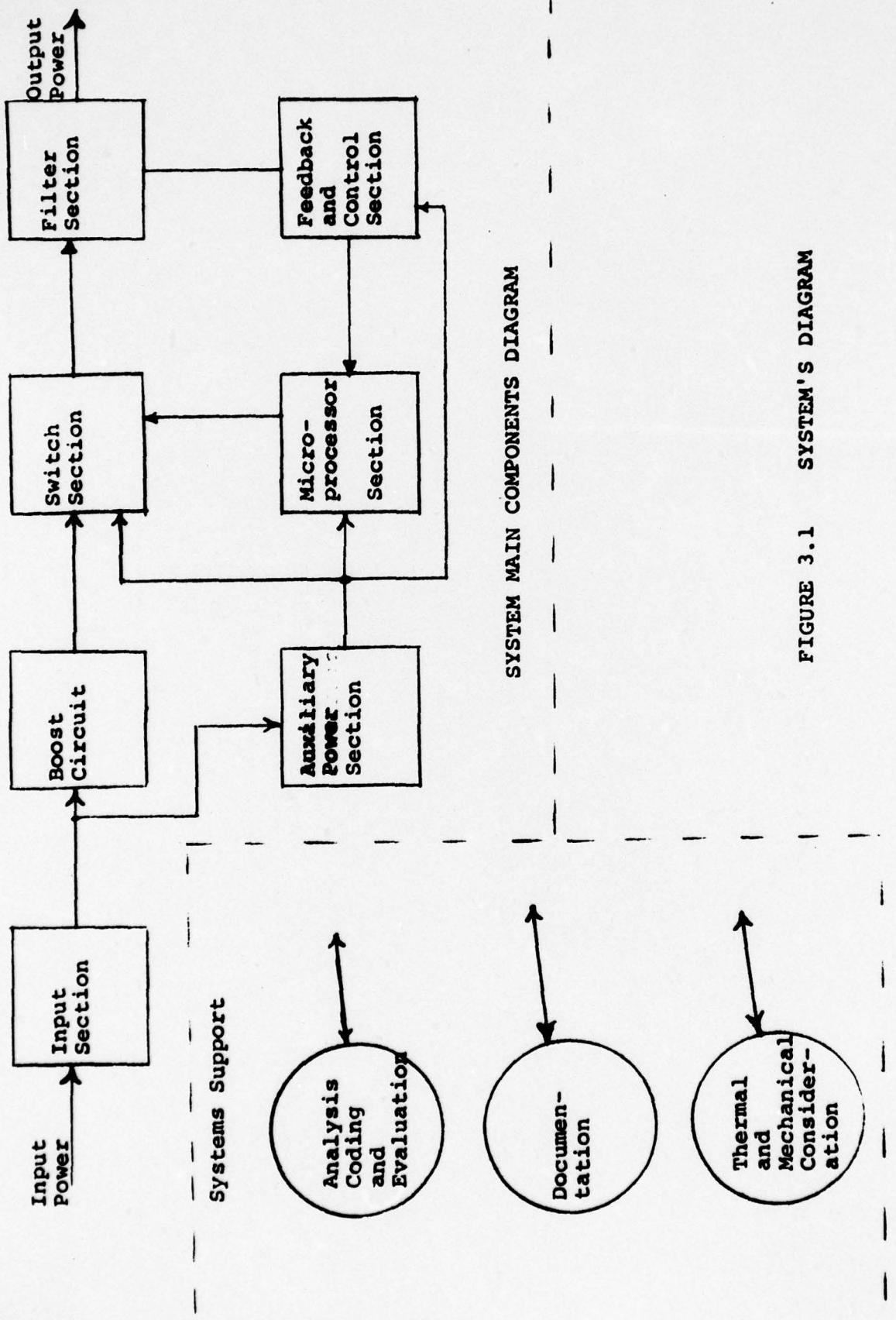


FIGURE 3.1 SYSTEM'S DIAGRAM

The poor quality, three phase, input signals are fed into the input section where they are rectified using a full wave three phase bridge to produce a split DC voltage supply. This split voltage is boosted using a boost circuit to achieve the desired ± 175 volts needed to produce the output power. Power conversion is accomplished using pulse width modulation (PWM) techniques. Microprocessor generated PWM signals are fed into USAMERDC Integrated Power Switch, manufactured by Texas Instruments, to control its "on time" thereby generating on an output current waveform which represents a sinewave.

The current sinewave is filtered using a low pass Tchebycheff filter to achieve a good quality, low distortion output voltage sinewave.

3.2.1 INPUT SECTION

A schematic diagram of the input section is shown in Figure 3.2.1. The input section consists of a three phase full wave rectifier bridge, over-voltage protection circuits, filter inductors, snubber networks and output filter capacitors.

Poor quality, unregulated, three phase, raw AC power is coupled into the input section via the three phase rectifier bridge producing an output voltage of normally 360 volts under no load and 280 volts under full load. Both of these voltages were calculated assuming an input voltage of 208 volts line to line. A 20 microhenry inductor L_2 , 3 , 4 has been incorporated into each input line to prevent generation of undue line to line current transients during rectifier diode commutation. Further protection of the bridge is achieved using snubber RC network R_1 , C_2 through R_6 , C_6 across each diode D_1 through D_6 in the bridge. The input power must be three phase but could be at any frequency from 50 to 1600 Hz. The drain on the output filter capacitors will be at 50, 60 or 400 Hz.

The average input current I_ϕ Avg has been calculated to be 51 amperes and the effective load resistance is 5.5 ohms. To account for load variations, system losses, etc., an effective load resistance of 4 ohms has been used for all calculations. With a 4 ohm load the average current is 70 amperes.

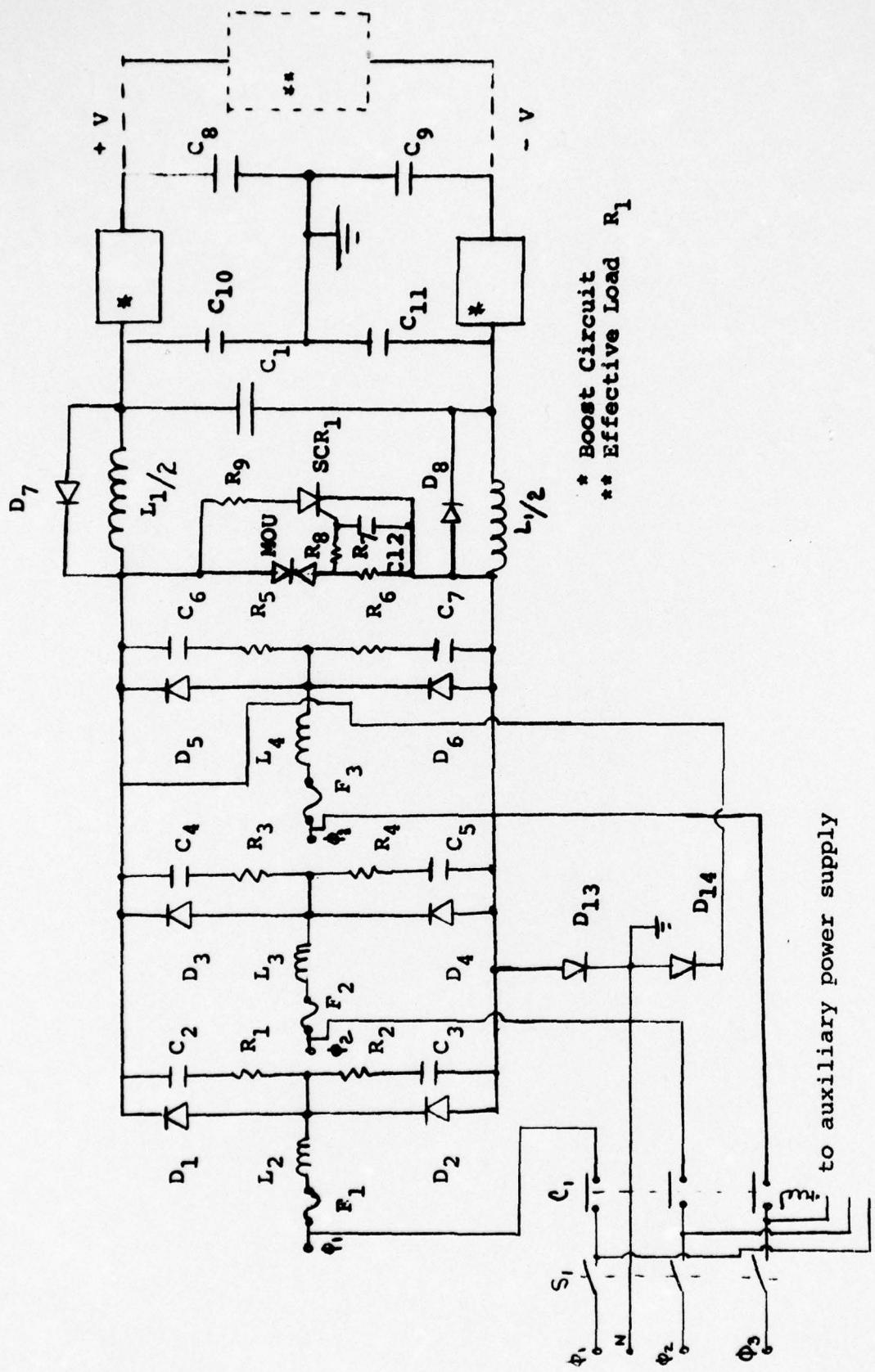


FIGURE 3.2.1 THE INPUT SECTION

It is commonly known that the actual input current from each phase is:

$$I_{\text{ph RMS}} = .816 I_{\text{AVG}} = 56 \text{ Amperes}$$

Henceforth, the worst case RMS input current per phase could be as high as 56 amperes.

Once the load has been determined the minimum input inductance can be determined. This inductance is found by (1)¹:

$$L_1 = \frac{k}{f_s} R_1 \text{ henrys} \quad (1)$$

Where: $k = 0.0017$ for a full wave three phase circuit

R_1 is the maximum load

f_s is the frequency of the source in Hz.

Assuming a worst case input frequency of 60Hz, the minimum inductance becomes 110 microhenrys.

After the inductance has been determined the filter capacitor is determined using the ripple factor formula (2)¹:

$$\gamma = (0.0079/L_1 C_1) (60/f_s)^2 \quad (2)$$

for and f_s of 60 Hz and a ripple factor of .1

$$C_1 = \frac{0.079}{L_1} = 718 \text{ Microfarads} \quad (3)$$

1) Reference data for Radio Engineers, fourth edition, International Telephone and Telegraph Corporation, 1956.

Filter capacitance C_1 , C_{10} , C_{11} of 5400 microfarads capacitor will be used thereby reducing the ripple factor to nearly 0.01 or 1%. Six of these capacitors will be used in order to achieve greater ripple current capability. Each of the 400 volt, 1200 microfarad capacitors has a ripple current capability of 7 amperes. This means that the total ripple current is 35 amperes. This current should be sufficient to smooth the input current ripple.

To enhance system reliability and to further reduce the ripple factor while providing extended ripple current capability, Sprague type 32D capacitors of the high energy type are used in the output filter bank. Each capacitor in this bank is 7000 microfarads at 100 volts. By using 8 capacitors on each side and using a center tap, the total output capacitance is further increased by 7000 microfarads thereby reducing the ripple factor to approximately 0.005 or 0.5%.

The filter inductor L_1 has been split into two inductors. One in the positive bus and one in the negative bus. Diodes D_7 and D_8 are used to prevent high voltage spikes associated with the collapsing fields of these inductors when the input power is removed. To further protect the bridge and other system components a crowbar circuit consisting of the MOV, R_9 , SCR_1 , R_7 , R_8 and C , has been incorporated to detect over voltage. If over voltage is detected SCR_1 will be turned on

clamping the output of the bridge through a 1 ohm 20 watt resistor R_9 . This action will most likely cause fuses F_1 , F_2 and F_3 to open. In any event this action will lower the voltage across the bridge significantly thereby protecting it and the USAMERDC switch which is rated at 400 volts.

The commutation time of the bridge $D_1, 2, 3, 4, 5, 6$ could be as long as 2 microseconds. With an input frequency of 1600 Hz the average current through Resistors $R_{1,2,3,4,5,6}$ could be as high as 0.3 amperes. If these resistors have a value of 3 ohms the power loss will be .27 watts. The value of these resistors is 3.3 ohms, one watt carbon resistor. The series capacitor has a value of a 0.068 microfarad capacitor. They are low ESR high frequency Sprague orange drop type capacitors.

In the above calculations no considerations were made concerning the effects of voltage boost. Voltage boost is discussed in Section 3.2.2

3.2.2 BOOST CIRCUIT

The raw AC input to the converter can vary + 10% and -15% when those variations are combined with the losses inherent in conversation, it becomes imperative that some sort of boost circuit be used to maintain the DC voltage at the

DC bus level of ± 175 volts. The voltage boost circuit also reduces input harmonics associated with the raw AC power source. The boost circuit also supplies substantial high frequency current pulses to reduce the need for excessive high ripple current capability of the split capacitor bank consisting of C_8 and C_9 as shown in Figure 3.2.1-1.

Some of the methods investigated to achieve reliable voltage boost include:

1. A fixed frequency variable PWM system.
2. A self-resonant fixed frequency variable output amplitude.
3. Low frequency (400Hz) combined boost and auxiliary power use separate boost at high frequency.
4. A variable frequency load dependent natural commutation interval.

When a fixed frequency is used with a variable pulse width modulation scheme, it is extremely difficult to have zero output from the boost. Zero output is absolutely essential under no load conditions, thus fixed frequency variable pulse width modulation was not selected.

A self-resonant fixed frequency variable output amplitude is extremely difficult to accomplish. It is very expensive and fairly unreliable. Additionally, it does not lend itself to zero boost. For these reasons a self-resonant fixed frequency was not selected for the boost circuit design.

A low frequency load dependent natural commutation interval could be used. However, if such a boost circuit is used the component needed such as inductors, capacitors and transformers are excessively large when boosting 5KW to 8KW. Thus, weight and system cost would not be consistent with the objectives of this program.

Additionally, at the power transfer levels required for this boost circuit, the acoustical noise would be unacceptable. When an attempt is made to maintain the operating frequency at 400 Hz such that the boost circuit can serve to generate fan motor drive and the auxiliary power, then a boost conversion of zero volts is not possible. For these reasons the auxiliary power and boost circuit are separate. Because of weight and cost requirements, a high frequency boost circuit was chosen.

A variable frequency load dependent natural commutation interval was selected as the best approach to meet the boost circuit requirements. It can provide zero volts boost which is absolutely essential. It operates at a high frequency (under load) thus small components are used. Two types of variable frequency load dependent natural commutation interval circuits were investigated. These two circuits are shown in Figure 3.2.2-1 and 3.2.2-2.

Figure 3.2.2-1 shows a variable frequency neutral reference boost circuit. Boost action starts when SCR₁ is turned on causing current flow through inductor L₅ and capacitor $\frac{C_{15}}{2}$ and C₁₅. Once capacitor $\frac{C_{15}}{2}$ is charged, SCR commutates, generating the first half of the output wave. The second half of the cycle is generated from the collapsing field of L₅. After this commutation action is complete, SCR₂ is turned on generating a sinewave which is 180 degrees out of phase with the previous wave generated by turning on SCR₂. The circuit is very efficient and highly reliable. Using RCA 2N3658's the circuit easily operates up to 20 KHz. In this circuit configuration, twice the current is needed to produce the required power. This is true because of the neutral reference. The need for diodes D₉ and D₁₀ as well as snubber networks R₁₀, C₁₃ and R₁₁, C₁₄ are presently in the design as a precautionary measure. Some of these devices may be eliminated in future designs. This design is somewhat simpler than that shown in Figure 3.2.2-2. However, this circuit must handle all of the power, while in the split capacitor arrangement. A three phase design can be used thereby providing a method of using low cost available pot cores. In the second case three 2KW transformers would be used while in the circuit shown in Figure 3.2.2-1 a single transformer capable of producing 6KW to 8KW is needed.

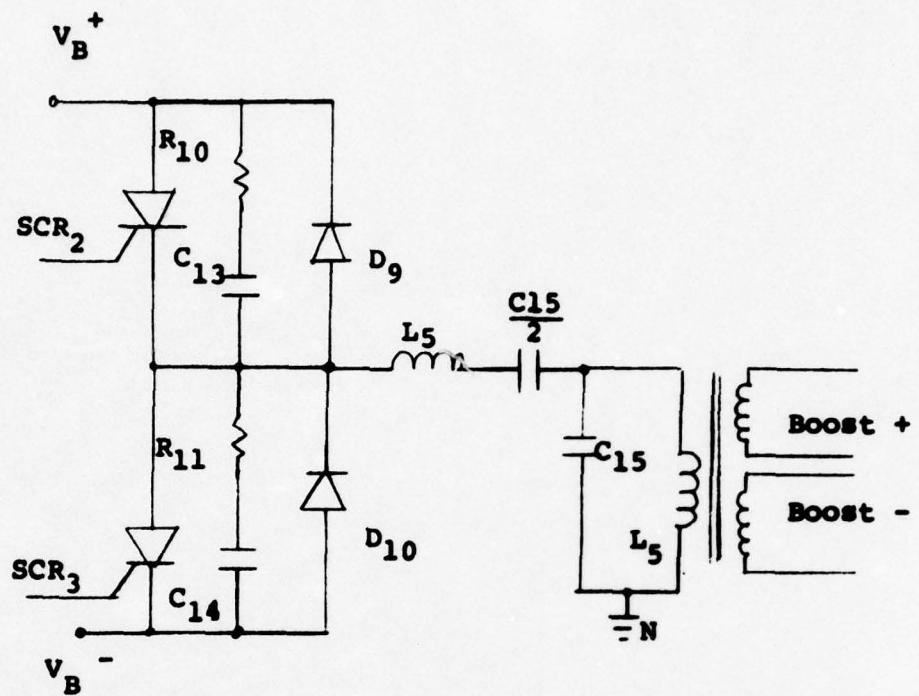


Figure 3.2.2-1 VARIABLE FREQUENCY NEUTRAL REFERENCE BOOST CIRCUIT

Figure 3.2.2-2 operates almost the same as that of 3.2.2-1 except that a split capacitor arrangement is used instead of the neutral reference.

Final circuit design which was breadboarded, tested and incorporated into the final system is identical to that of Figure 3.2.2-2. When SCR_4 is turned on, voltage is applied to L_6 causing a change in its flux which in turn allows for a change in current eventually causing capacitor C_{18} and $\frac{C_{18}}{2}$ to charge up. Once C_{18} and $\frac{C_{18}}{2}$ are fully charged and no more change in voltage occurs across them, the field of the inductor collapses causing current flow in the opposite direction commutating SCR_4 off. The second half of the cycle is accomplished in a similar manner using SCR_5 , inductor L_7 , and capacitor C_{18} combined with $\frac{C_{18}}{2}$. Continuation of alternate pulse trains to SCR_4 and SCR_5 allow for the production of a sinewave at the natural frequency of the tuned circuits. Test results show that this circuit operates satisfactory over a drive frequency from 1 KHz to 22 KHz. Naturally, maximum power transfer occurs at 22 KHz while very little power transfer occurs at 1 KHz. By using a VCO to generate the alternate pulse train to drive the SCR's regulation is supplied for the boosted output.

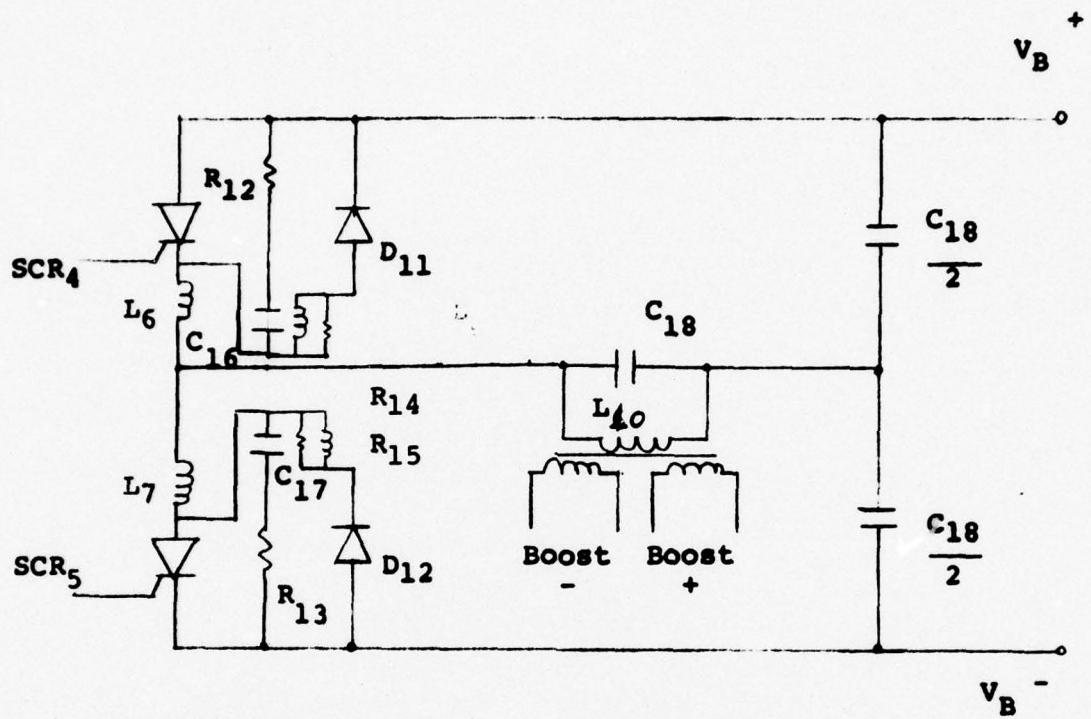


FIGURE 3.2.2-2 VARIABLE FREQUENCY SPLIT CAPACITOR BOOST CIRCUIT

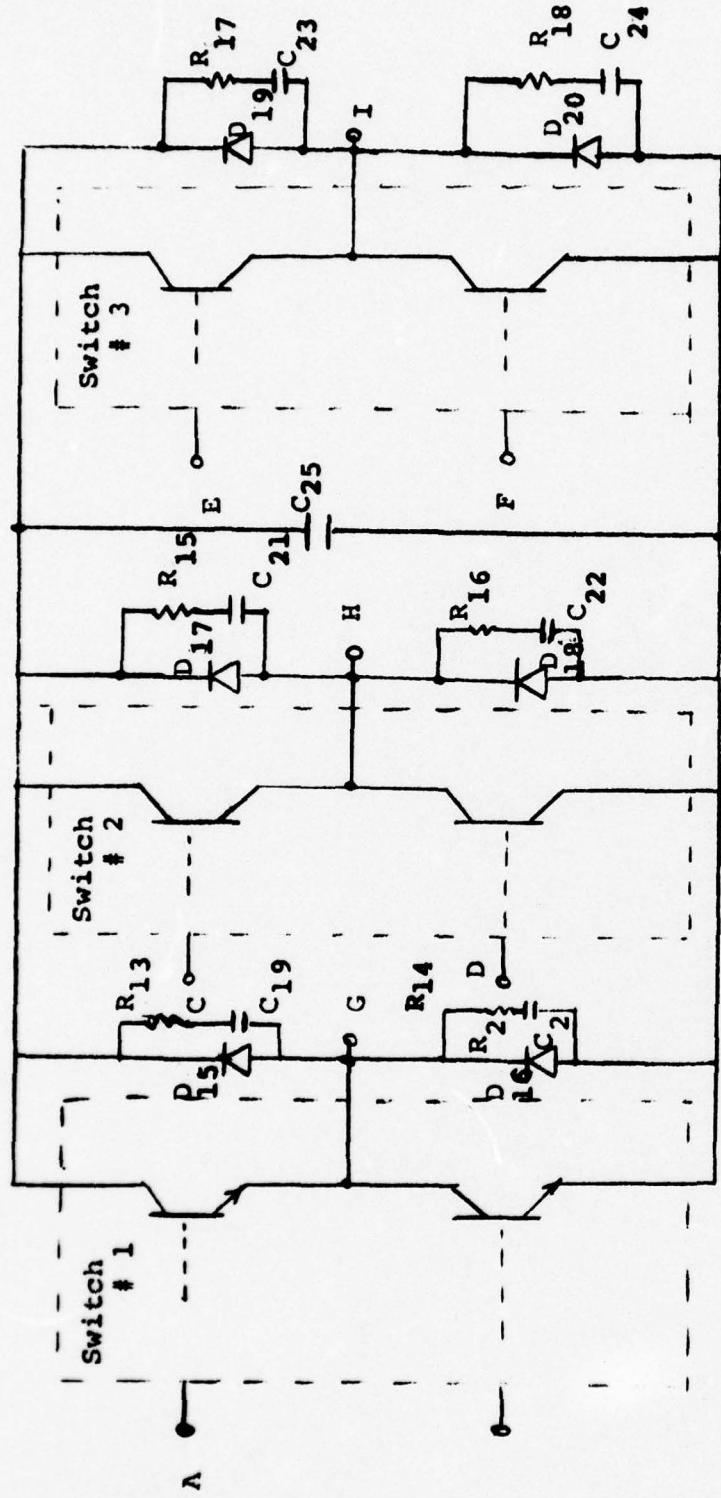
3.2.3 SWITCH SECTION

A schematic diagram of the switch section is shown in Figure 3.2.3-1. The switch section consists of three USAMERDC Integrated Power Switches manufactured by T.I., rated at 400 volts and 100 amperes. The switch operates from TTL Signals and will reliably operate at frequencies up to 10 kilohertz. Freewheeling diodes D₁₅ through D₂₀ are connected external to the switches. The purpose of these diodes is to protect the switch against large reverse current and voltage spikes. As further protection snubber networks R₁₃C₁₉, R₁₄C₂₀, R₁₅C₂₁, R₁₆C₂₂, R₁₇C₂₃ and R₁₈C₂₄ connected across each switch.

The switch operates best from a low impedance source. It must also have substantially wide current carrying conductor to reduce "skin effect". Good high frequency, low ESR, capacitor must also be used across the voltage bus to suppress generated noise.

The switching arrangement shown in Figure 3.2.3-1 is sufficient to generate the required three phase output. In order to achieve good quality power the switches must be driven using a suitable and proportional sinewave pulse width modulated (PWM) signal into the base of each switch.

An analysis and description of the drive pulse train is provided in Section 3.2.8.



A, B, C, D, E and F are PWM inputs
 G, H and I are switch outputs to appropriate filter inputs

FIGURE 3.2.3-1 THE SWITCH SECTION

3.2.4 FILTER SECTION

The output filter is used to convert the pulse width modulated waveform to its fundamental sinewaves. This is accomplished by stripping out the carrier frequency with a low pass filter which has a corner frequency far below the carrier frequency. While the corner frequency of the filter must be substantially below the carrier frequency, the corner frequency must not be so low as to cause a significant alteration of the output voltage sinewave.

Ideally, the output impedance of the filter should be fairly low to accommodate load variations without significant variations in the amplitude of the output voltage sinewave. Small variations are easy to regulate using feedback to close the loop.

Another criteria which must be met is to minimize the real voltage drop across this series elements in the filter. While series drop must be small to prevent undue losses, the reactive impedance must be large enough to limit the di/dt of the switch to a reasonable level.

A schematic diagram of the output filter networks is shown in Figure 3.2.4-1. This schematic shows the filter required for all three phases. The filter for each phase uses two low pass filters (Tchebycheff Type). The first section of the filter consists of $L_{12}L_6C_{25}$, $L_8L_{13}C_{27}$ and $L_{10}C_{29}L_{14}$. The purpose of this filter is to reduce the effects of carrier frequency ripple.

The main filter of each filter section consist of L_7C_{26} , L_9C_{28} , and $L_{11}C_{30}$. Typically the corner frequency of this filter is set at the third harmonic of the fundamental. Ideally, this carrier frequency will be set at 1200Hz which is the third harmonic of the 400Hz fundamental and the harmonic content of the wave is maintained by increasing the pulses per half-cycle.

A detail analysis of the filter section is given in the mathematical analysis section 3.2.8.

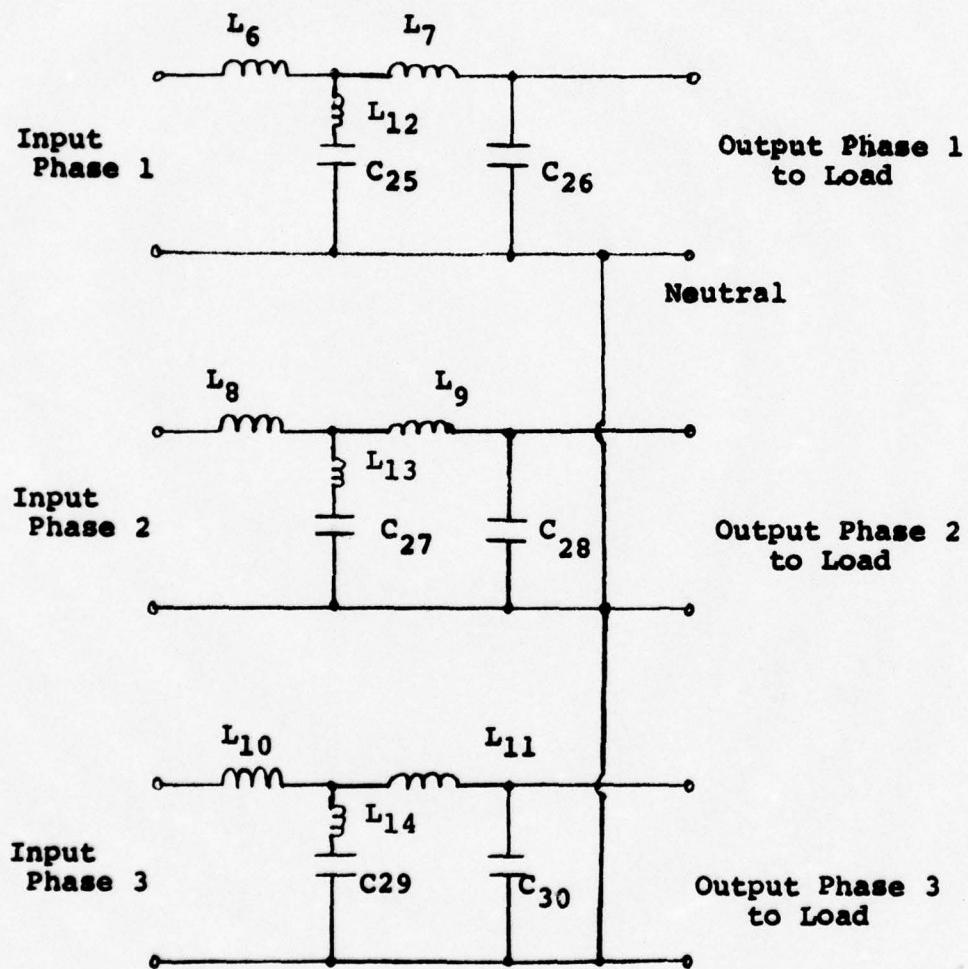
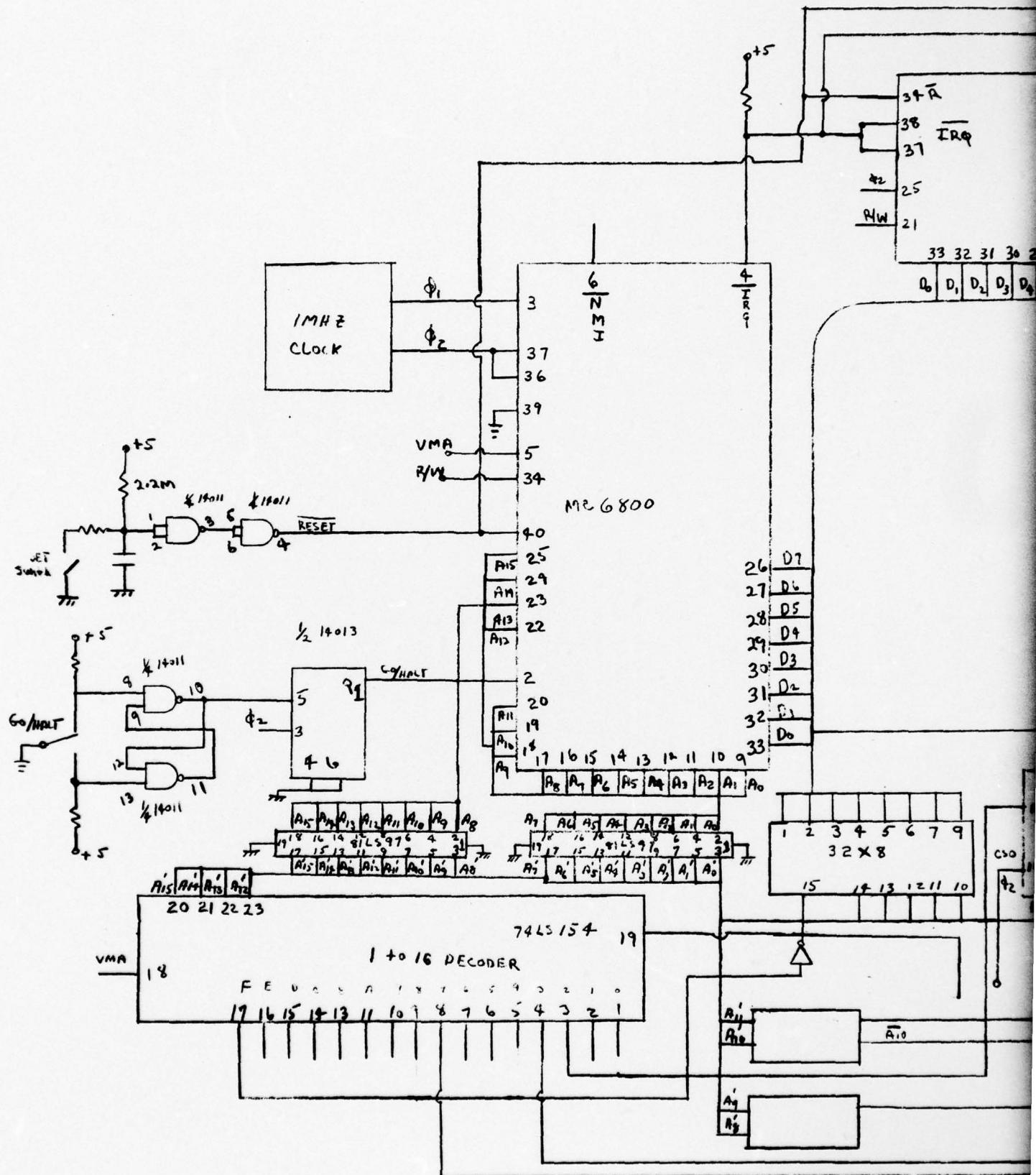
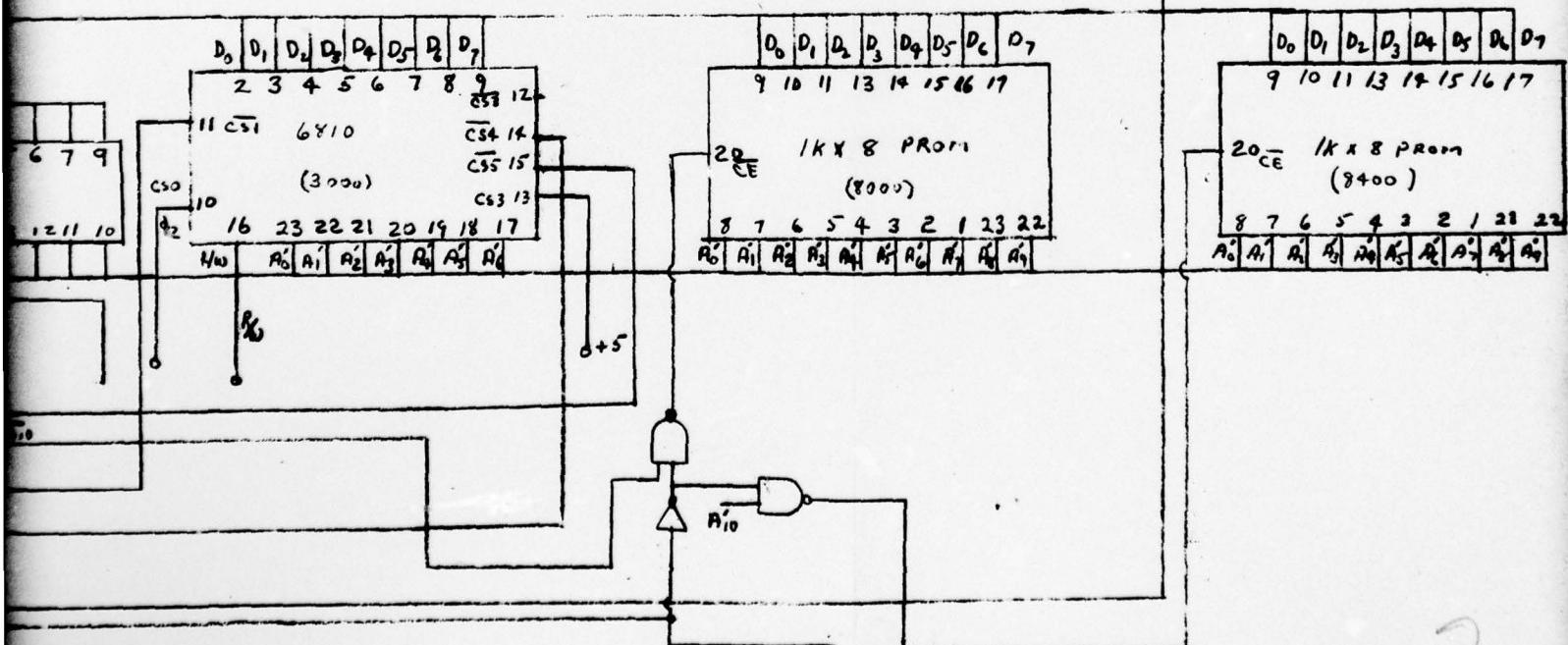
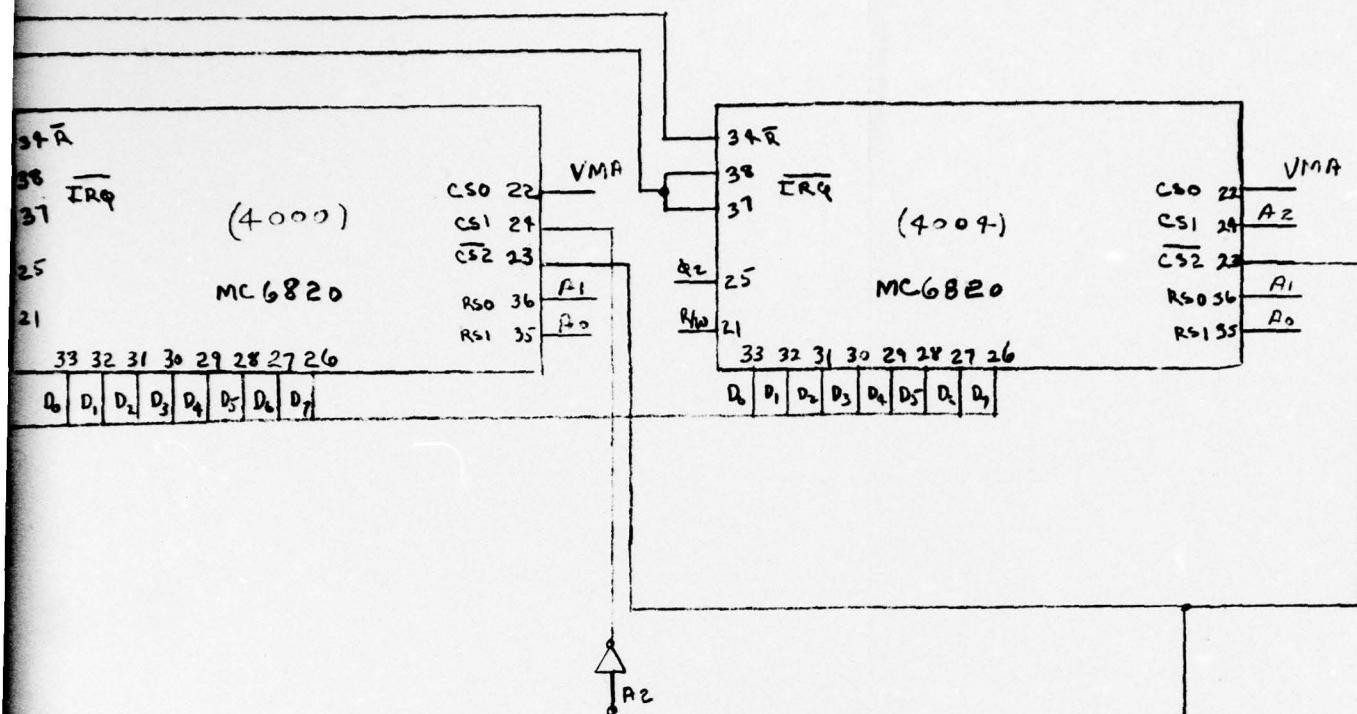


Figure 3.2.4-1 THE FILTER SECTION FOR THREE PHASES

3.2.5 THE MICROPROCESSOR SECTION

Several methods avail themself for the control, analysis processing and generating of signal to the power section of the converter. These methods include discrete logic (transistors, resistors, capacitors, etc.), integrated logic (gates flip flops and small scale logic devices on chips) and large scale integration (LSI). As the state of the art in semiconductors continues, the number of devices on a chip continue to increase from two to four thousand devices in 1972 to over 10,000 devices in 1976. Evolving from this large scale integration are sets of chips which when properly used can substantially reduce discrete and integrated logic at a reduced cost, smaller size and a higher reliability. In general, these LSI chip sets are called "microprocessors". However, in some cases they are referred to as microcontroller and microcomputer. These units which are "computer on a chip" are capable of rapidly processing information, controlling and monitoring devices and actions and, based upon processed data, generate the correct output signals to control most any device or system. In this research effort an MC6800 microprocessor has been chosen. Basically the MC6800 microprocessor chip set consists of a MC6800 processor (MPU), an MC6820 peripheral interface adapter (PIA), a MC6810 Random Access Memory (RAM) and a MC6830 read only memory (ROM).





The system used in this effort uses 1 MPU, 2 PIA's, 1 RAM and 2 ROM's. To facilitate development, the ROM's will be replaced by programmable read only memory (PROM's).

A schematic diagram of the microprocessor section is shown in Figure 3.2.5-1. When power is turned on the MPU generates a start vector (at the top address in the system) which serves to initialize the system. First it generates all data for the pulsewidth modulation of all three phases and stores it away in a buffer (not shown in this figure). Then it monitors all response signals to determine that enough pulses exist per half cycle to guarantee a good quality low distortion sinewave at the desired frequency. Additionally it updates the buffers as changes occur. The program in the processor (PROM) has the capability of changing pulses per half cycle, controlling the output frequency, dynamically controlling the output amplitude and exactly controlling the phase shift to adapt the system to any load.

The system shown in Figure 3.2.5-1 has fully decoded addressing, restart, interrupt, reset and go/halt capability. The system uses a 1 megahertz clock to generate the two phase clock signals ϕ_1 and ϕ_2 .

The memory address allocation in Hexadecimal is as follows:

1 to 7FF	Buffer area
800 to 2FFF	Not used
3000 to 30FF	Scratch pad area
3100 to 4000	Not used
4000 to 4003	PIA # 1
4004 to 4007	PIA # 2
4008 to 7FFF	Not used
8000 to 83FF	PROM # 1
8400 to 87FF	PROM # 2
8800 to FFE0	Not used
FFE0 to FFFF	Restart and interrupt PROM

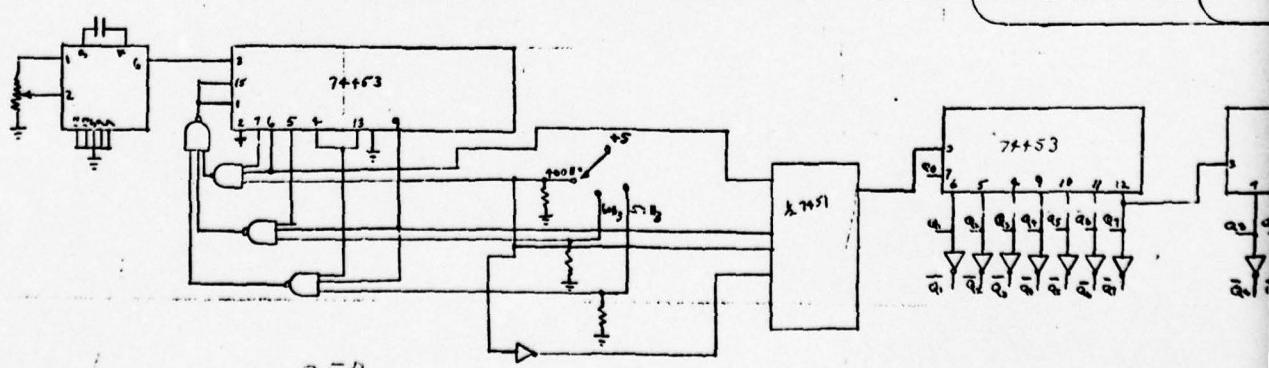
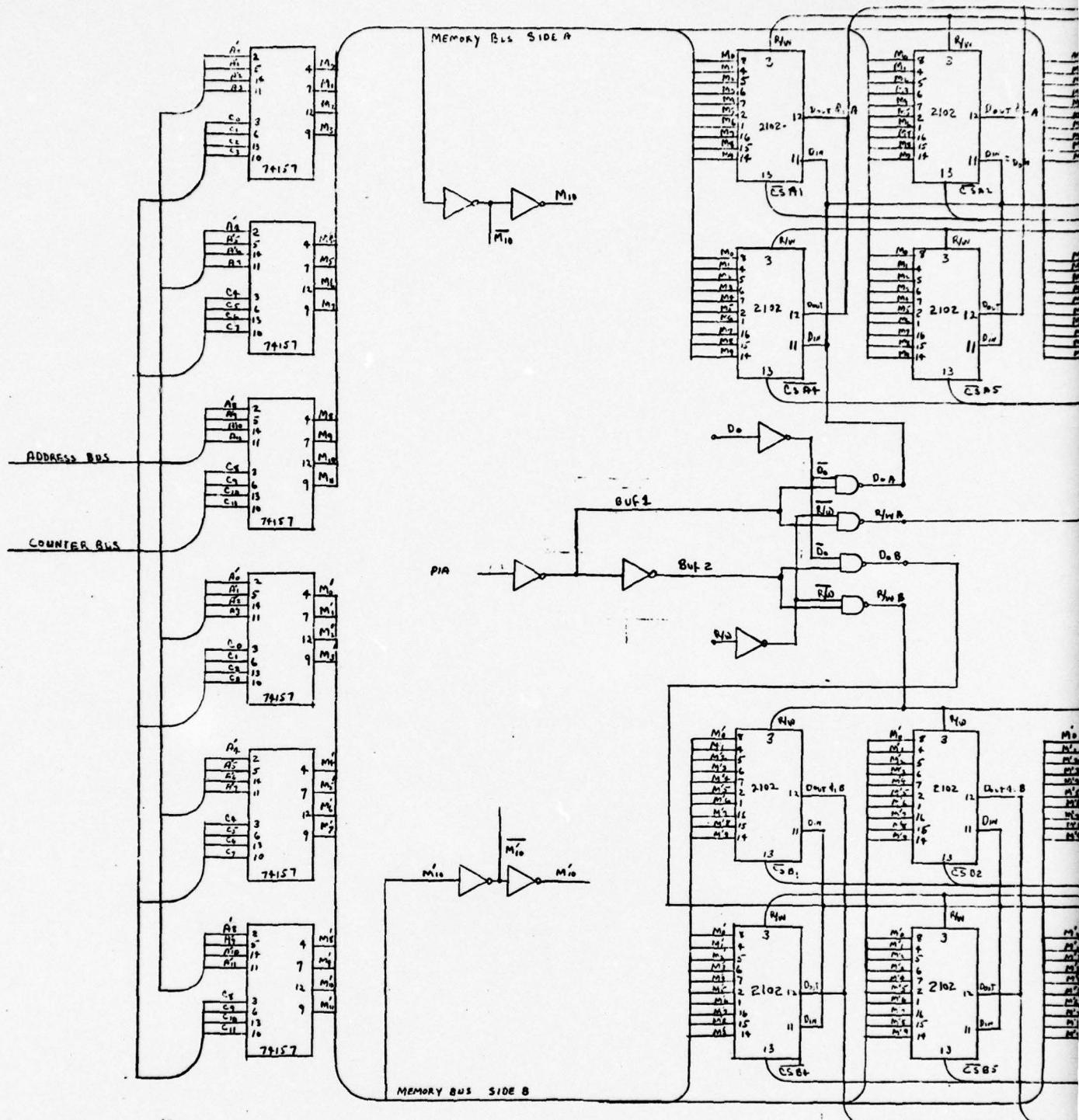
The MC6800 is an 8-bit processor system. Its repertoire of executable instructions is 72. These instructions are executed by the MC6800 using its two accumulators, its index register, its stack pointer and its program counter.

The machine operates as follows:

At start up the processor sends out an address FFFE and FFFF. The 32x8 Prom at the top address is enabled by this address thereby causing two bytes of data to be sequentially placed on the data bus and thus received by the MPU. These

two bytes of data become the 16 bit vector address to tell the MPU where it should next read data (start execution). The 16 bit vector address becomes the new program counter value which is sent out to the address bus as soon as the processor has stabilized. All execution of external addressing is sync with clock signal ϕ_2 . The processor now continues to operate based upon the instructions that it receives. Its operation at this point is much like that of a mini-computer. Probably, the primary difference between its operation and that of a mini-computer is that its execution is accomplished from PROM rather than RAM or core memory and the fact that most mini's use 12 and 16 bits instruction words.

The final portion of the microprocessor section is the buffer. A schematic diagram of the buffer (called high granularity pulse width modulation generator) is shown in Figure 3.2.5-2.



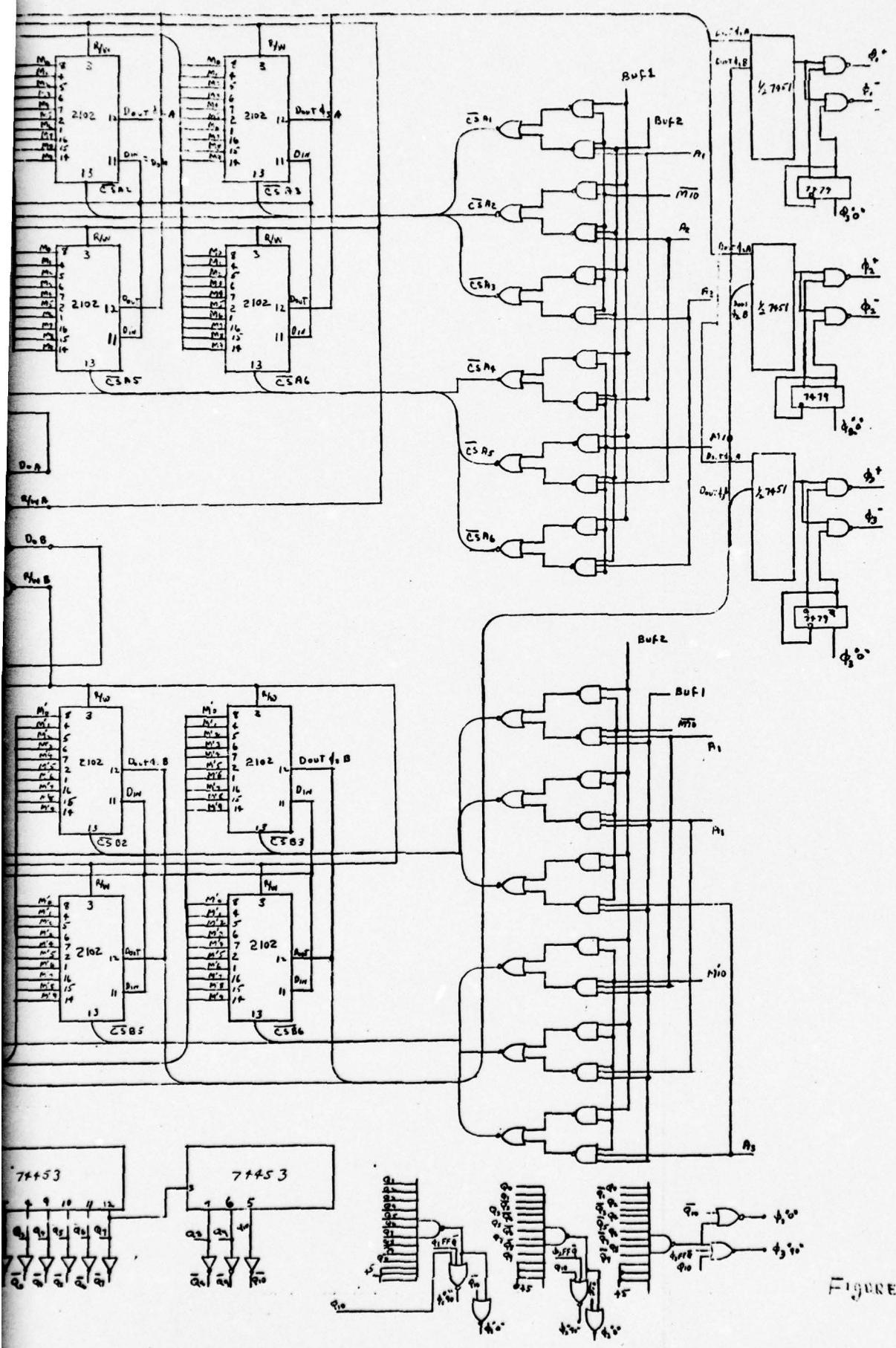


FIGURE 3.2.5-2 THE ZILLER

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This buffer arrangement was chosen to:

1. Facilitate rapid updating of the code due to changes in the load.
2. Allow for easy operation of the switch at almost any frequency from almost zero to approximately 1000 Hz.
3. Provide complete flexibility to the processing and the control of various feedback parameters.
4. Allow the potential of programming the desired output voltage to almost any output level.
5. Provide for output voltage shaping.

The buffer system is the heart of the PWM controller.

It serves as a free running interface between the microprocessor and the power switches. Actually, the buffer is a double buffer arrangement where one buffer is working with the power switch while the other buffer is used to update the PWM signals due to load variations. Upon command from the processor and at the proper time in the power interval either buffer can be selected to operate with the power switch.

The buffer system consist of two distinct sets of memories per phase. Each memory set is 2048 location long consisting of two 2102 type, 1024x1, static memory. The buffer is set up such that while one memory set is being read using an eleven bit ripple counter the other memory set for the selected phase is being updated by the microprocessor. As mentioned above the memory address for this buffer is at zero. A zero address was selected to enhance coding of the software.

The output of the memories addressed by the ripple counter are coupled into an output drive circuit which through proper gating allow for the selection of the desired switch to be driven.

Other methods of controlling the output power interface from the processor to the switch were considered but were rejected. These methods included direct drive from the processor which is obviously more desirable. However, it was felt at the time the computing power necessary to control system parameter and the need for maximum flexibility made the described method the most desirable. The present method is economical, reliable and small in size.

3.2.6 FEEDBACK AND CONTROL

3.2.6.1 SAMPLING

The determination of the feedback and control inputs are accomplished using sample and hold techniques. Essentially, the same method is used to determine leading and lagging power factor, peak voltage, and peak current (power).

At zero degrees of the drive waveform and its resulting current waveform (using a current transformer at this point) is sampled for leading and lagging power factor by the polarity of the sample. The magnitude of the lead or lag power factor is determined by the amplitude of the sample wave. Thus, the amplitude of the sample is proportional to the degree of phase shift introduced by the load.

Once the leading or lagging power factor has been corrected by forcing the current and voltage to be in phase, then the amplitude of the output voltage is monitored at ninety degrees of the drive waveform to control the output voltage to 120 VRMS from line to neutral. It must be recognized that there are inherent delays between the drive voltage crossing and the generated or measured waveforms. The inherent delays or phase shifts are system constants which are easily nulled out.

In an orderly sequence, 1st phase shift is connected, then output voltage, then power and finally ripple distortion.

Power will be controlled by determining the current amplitude at ninety degrees of the drive waveform. Power correction is accomplished by adjusting (proportionately) each pulse in the drive waveform.

The ripple distortion can be made by using a high pass filter with half wave rectification of the passed signal to obtain a D.C. result proportional to the ripple factor.

When these signals are continuously sampled at the zero and ninety degree points with hardware decoding, the processor assesses this information asynchronously, as required, through peripheral interface adapter (PIA) and a controlled multiplexer.

The above discussion provides an indication of the various feedback parameters that are controlled.

A schematic diagram of the feedback section is shown in Figure 3.2.6-1. Each phase has a voltage detector, a peak voltage detector and a crossover detector. Monitoring of the output is accomplished through the use of an optical coupler which feeds the sample and hold, crossover detector, and the peak detector.

The sample and hold is a simple boxcar circuit which samples upon command the analog input voltage and stores the sample as a voltage level on capacitor C₁₀₀. A source follower buffers this output. The output of the source follower is coupled into the analog to digital converter where it is converted to a digital word for use by the processor.

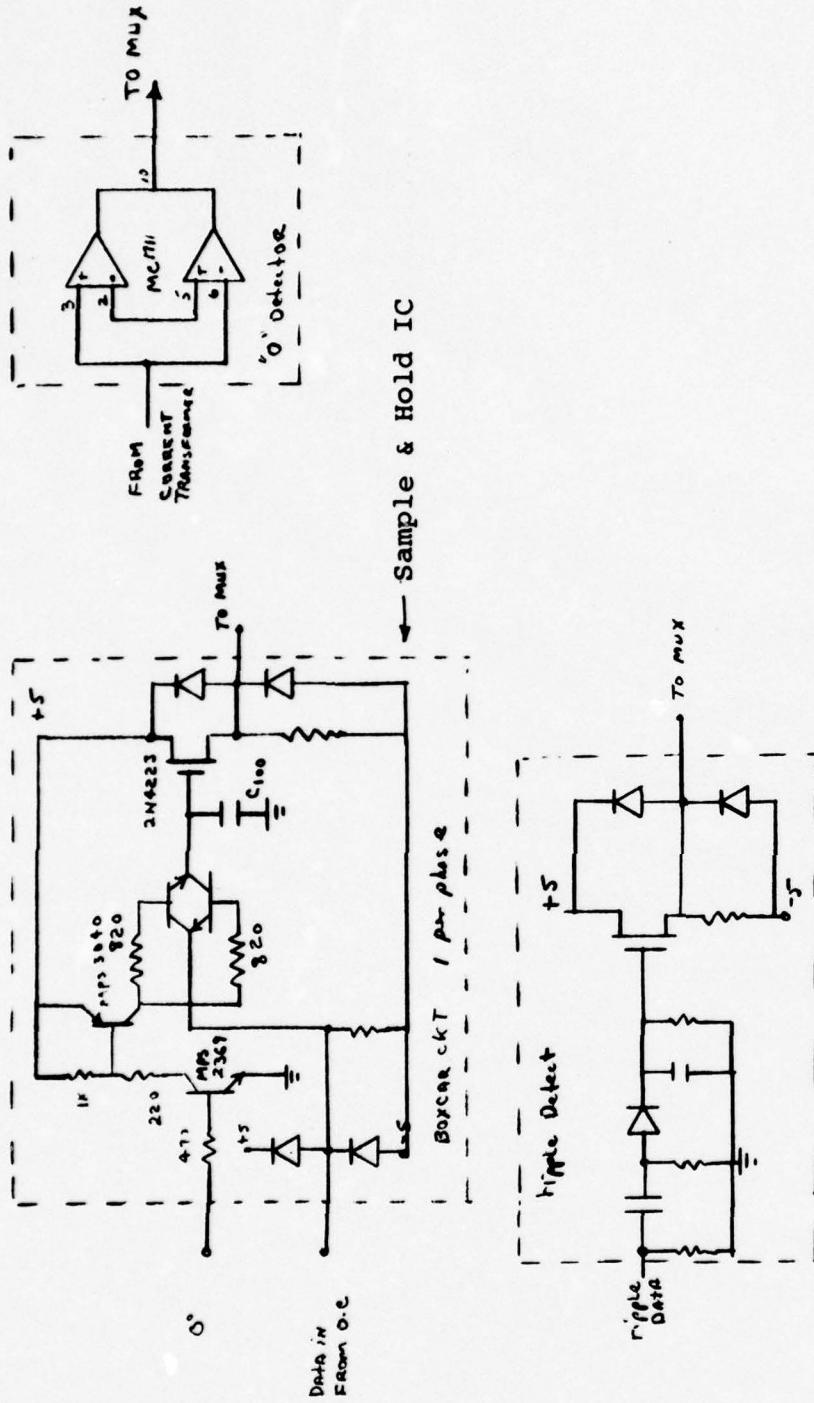


FIGURE 3.2.6-1 VARIOUS DETECTOR CIRCUITS FOR FEEDBACK AND CONTROL

3.2.6.2 CONVERSION

Conversion is accomplished using an analog to digital converter. It receives analog input signals and converts them to digital equivalents for use by the processor. A schematic diagram of the analog to digital converter is shown in Figure 3.2.6-2.

The analog to digital used is of the successive approximation register (SAR) type. This technique uses a digital to analog converter in a feedback loop to generate a known signal to which the unknown analog sampled signal is compared, and the comparator output controls the successive approximation register.

At the start of conversion the most significant bit of the D to A is turned on by the SAR, producing an output equal to half of the full scale value. This is compared to the sampled analog output and if the D to A is greater the SAR turns the MSB off. If it is less the MSB is left on. The next MSB is compared to the input unknown the same way, and in succession until the least significant bit is tested.

Since an 8 bit SAR and the clock signal is $\frac{\phi_2}{2}$ or 500 K Hz. The time to determine the digital equivalent of one sampled signal is 16 microseconds.

The microprocessor via the PIA 'A' register controls which of the sampled signals are to be converted, starts the conversion with an output pulse to the start conversion (S.C.) input of the SAR, and after receiving an End of Conversion (E.O.C.) signal reads the digital result of the conversion from the PIA 'B' registered.

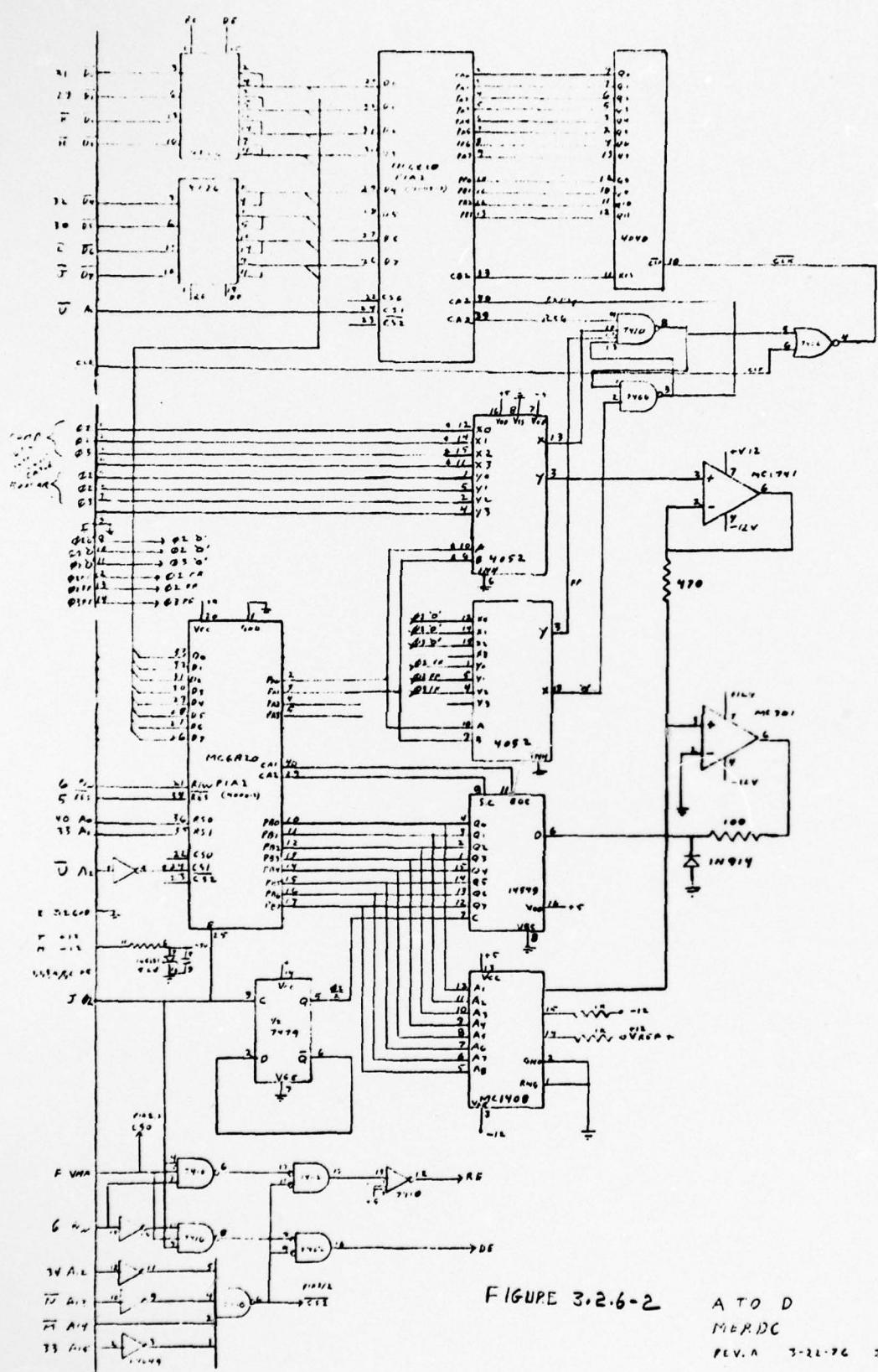


FIGURE 3.2.6-2

A T O D
M E P . D C
P E V . A 3 -

3.2.7 CODE EVALUATION AND ANALYSIS

3.2.7.0 INTRODUCTION

The software has been kept as generalized in structure as possible. This allows for the maximum incorporation of new features as they are developed. Calculations are made to the greatest accuracy the algorithms and microprocessor can achieve, to minimize round-off error and to retain the greatest number of significant digits in all respects. For example, the use of a multiply function is minimized and eliminated where possible. Instead of calculating the integral of the sine function between two angles, a table of data was generated using a calculator with 14 digit accuracy, which produces far more accurate results than 16 bit calculations (fixed point) can produce. An algorithm that the MC6800 could use to calculate acceptably accurate sinewave intervals might save about 200 bytes of memory now used in the sinewave integral table.

3.2.7.1 PRODUCING SINUSOIDALLY MODULATED PULSES

This effort involves the development of digital hardware and software to drive an Integrated Power Switch (IPS) that is connected to a source of D.C. with a sinusoidally modulated pulse sequence. The output of the IPS is then low-pass filtered to achieve a low distortion sinewave. The method of producing a sinusoidally modulated pulse sequence is accomplished by dividing a half-cycle into an odd number of intervals. During each interval, a pulse will occur that is centered in the middle of this interval. The width of each pulse is proportional to the integral of the sinewave function from the leading edge of the interval to this trailing edge of the interval. Therefore, an interval near the zero-crossing of the half-cycle will contain a narrow pulse and an interval near the maximum amplitude region of the half-cycle will contain a wider pulse. This method differs from an ideal sinusoidally modulated pulse sequence in that the software places the pulse in the center of an interval rather than centering the pulse at the point in the interval that divides the area of the integral in half, such that half the area under the integrated sine segment is on each side of this pulse center. Using this method, data for 1/4 of a cycle can be used to generate pulses for an entire cycle. Centering this pulse in the center of the interval has provided acceptable performance.

3.2.7.2 PULSE NUMBER FOR HALF-CYCLE

Due to the time constant of the low-pass output filter, a ripple voltage occurs on the output. The frequency of the ripple voltage is primarily determined by the number of pulses per half-cycle in the sinusoidally modulated pulse sequence. The ripple voltage can be reduced by two methods, with each method reducing overall efficiency in different ways.

The easiest way to reduce the ripple voltage is to increase the number of pulses per half-cycle, which increases the frequency of the ripple voltage with respect to the corner frequency of low-pass output filter. The change in pulse number per half-cycle is currently accomplished under program control. Feedback circuitry is being provided that will allow the magnitude of the ripple voltage on the output to determine the number of pulses needed per half-cycle to keep the ripple within specifications. If the pulse number increases or decreases, a slight adjustment in the amount of power being delivered to the load may be necessary to compensate for the increase or decrease in switching losses.

The second way to reduce the ripple voltage is to move the break (corner) frequency of the low-pass output filter closer to the fundamental frequency. This method is very effective in reducing the ripple voltage, but has a significant disadvantage due to the increased attenuation of the fundamental frequency. An advantage is that switching losses are not

changed. Also, switching this output filter corner frequency involves more inductors, longer current paths, switches and other hardware.

3.2.7.3 PULSE WIDTH MODULATION

In order to change the power delivered to the load by the sinusoidally modulated pulse sequence, the width of each of the pulses are multiplied or divided by a constant value. The software implements a change in power using divides only to retain accuracy and minimize round-off error. The length of the current random-access-memory used to store the data for generating the pulse sequence is 2048 bits. The number of bits per pulse interval is found by dividing 2048 by the desired pulse number per half-cycle. Any remainder from this division is added back into the data by a round off error correction routine. For a given number of pulses per half-cycle, each interval contains a relative number of the 2048 bits.

Of the bits in an interval, some in the center will be "on" bits, and the rest will be "off" bits. As the power per half-cycle is increased, there will be proportionally more "on" bits than "off" bits. After all the "on" and "off" bit distributions for each interval are calculated, then the round-off error correction routine determines if the data for all the "on" and "off" bits adds up to exactly 2048.

If there is a correction to be made, bits are added to or subtracted from the "on" part of each pulse interval starting at the outside interval and working towards the center pulse, starting at the outside again if there are more correction bits than intervals per half-cycle. When the correction factor was odd, 1 bit is added to or subtracted from the center pulses "on" value. In general, the number of correction bits appear to be between 1 and 1-1/2 times the number of pulses per half-cycle, which is about one-half of the number of times that round-off error can occur. Round-off error correction is important since errors in pulse widths or pulse locations in the sequence could introduce hard to eliminate distortion, and could introduce unwanted phase shifts.

3.2.7.4 PULSE BIASING

It was soon determined that the purely sinusoidally modulated pulse sequence would not achieve the lowest distortion sinewave. By experimenting, it was found that the sinusoidal modulation technique required to achieve low distortion involved reducing the amplitude of the original sinusoidal data and adding a constant factor to each table value which resulted in more of the "on" time per half-cycle being placed

further from the center of the half-cycle. This is probably necessary due to impedance losses and switching losses in the output filter, and possibly due to impedance in the source. That is, as the pulses get narrower going out from the center pulse, the losses per pulse become a greater percentage of the pulse's "on" value, which probably reflects the fact that the power loss per pulse is relatively constant.

3.2.7.5 PHASE SHIFT CONTROL

In order to provide feed-forward and feed-backward capability when the load has either leading or lagging power factor, a means of shifting the power center of the pulse sequence within a half-cycle by means of a single parameter is available in both hardware and software form.

Phase shift control is accomplished by effectively rotating the pulse data in the 2048 bit memory. Rotating displaces the center of the pulse sequence with respect to the zero crossing points of the half-cycle. Bits that were on one end of the pulse sequence are shifted to the other end. The program parameter that controls the rotating will be generated by circuitry that samples the phase between the current and voltage in the output.

3.2.7.6 GENERATED PWM SIGNALS

The ideal pulse width modulation scheme is shown in Figure 3.2.7.6-1. In this scheme pulses are generated for the positive half-cycle from the positive reference to ground to produce the positive half-cycle of the sinewave. Similarly, pulses are generated from the negative reference to ground for the negative half-cycle of the sinewave.

After much testing (as shown in section 3.2.7.7), it was determined that unless the input impedance was stabilized then regulation versus load could not easily be achieved. Consequently a scheme was selected to always have either one switch or the other switch on. The wave now generated is diagrammatically shown in Figure 3.2.7.6-2.

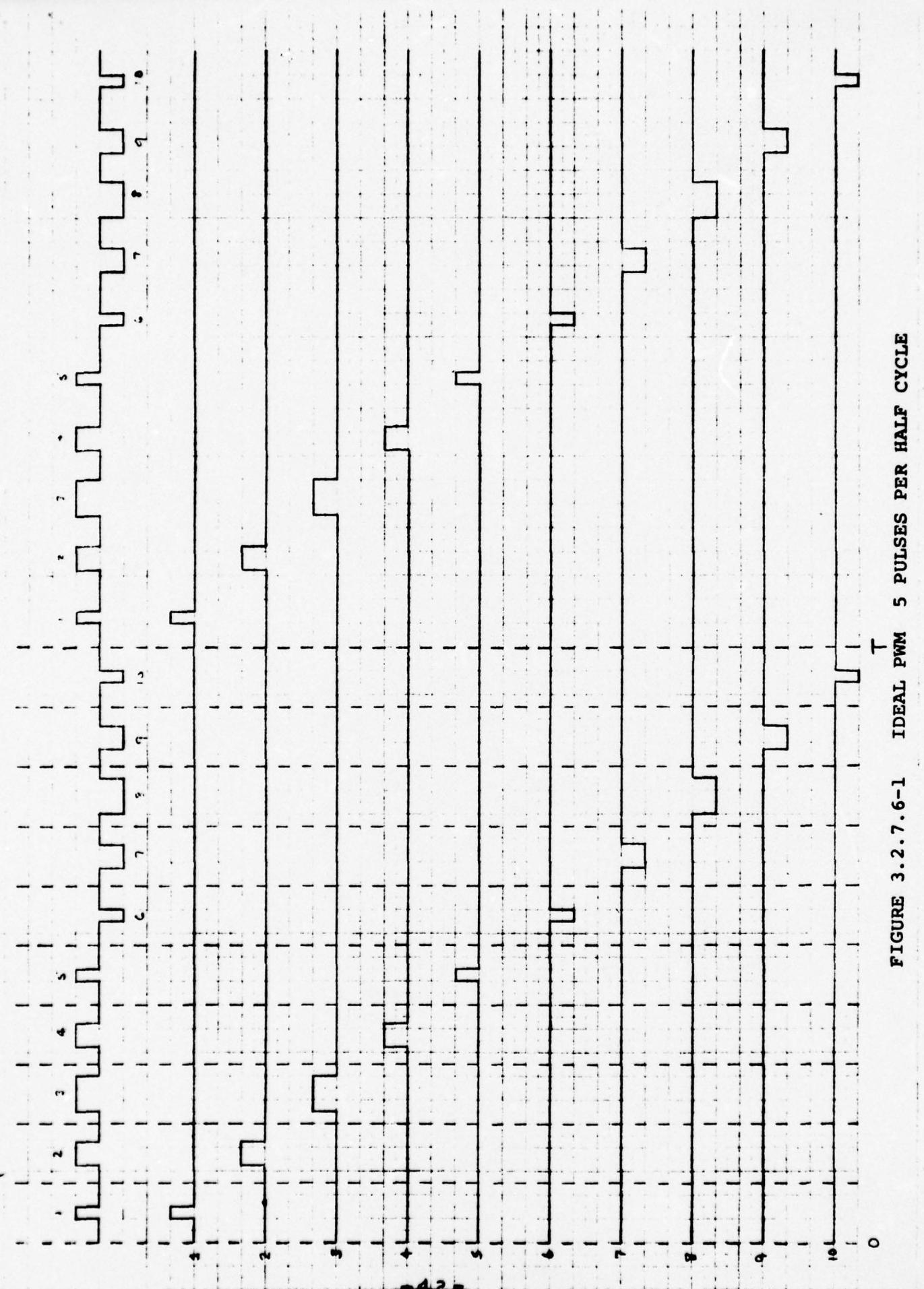


FIGURE 3.2.7.6-1 IDEAL PWM 5 PULSES PER HALF CYCLE

IDEAL PWM 3 PULSEs
PER HALF CYCLE

SWITCH A ON FOR NEW
PWM

SWITCH B ON FOR NEW
PWM

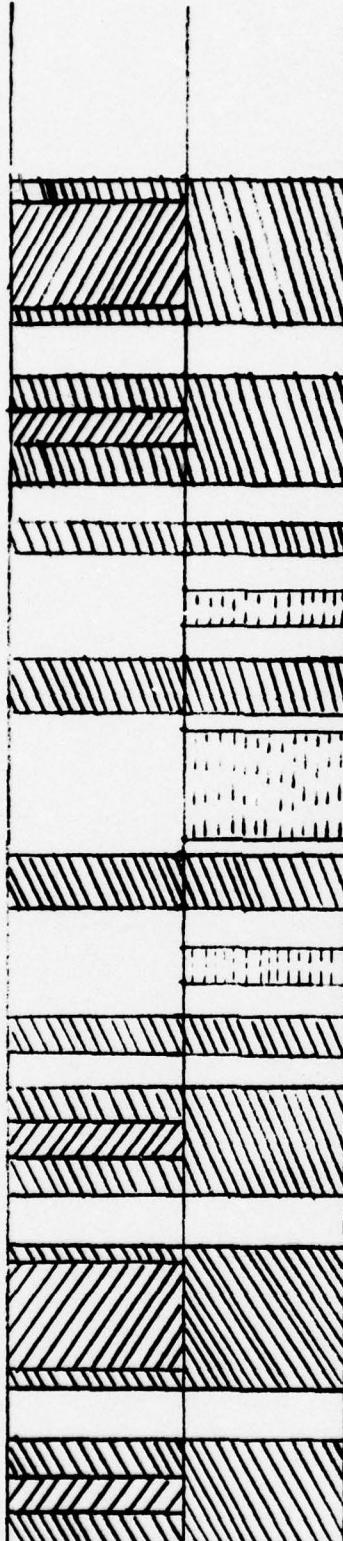
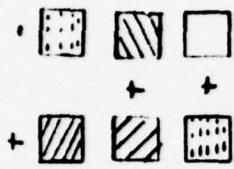


FIGURE 3.2.7.6-2 NEW PWM APPROACH

3.2.7.7 PERFORMANCE ANALYSIS

3.2.7.7.1 50 and 60 Hz OPERATION

A waveform that is within the specifications for ripple and distortion for 50 and 60 Hz frequencies has been achieved with an output filter with a corner frequency of 180 Hz. The power delivered to the load was 1800 watts with 51 pulses per half-cycle.

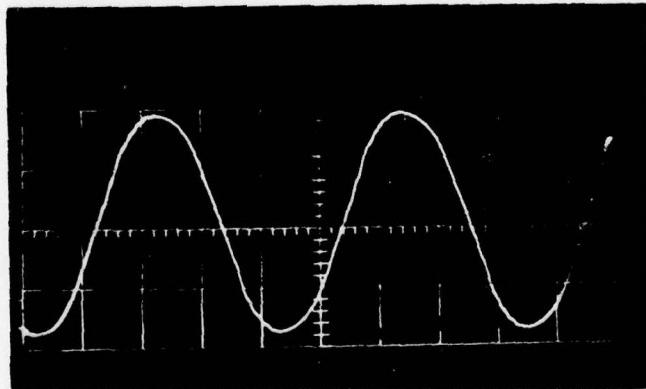


Figure 3.2.7.7

**60 Hz sinewave into 2 ohm load
using 1st method of PWM**

3.2.7.7.2 400 HZ OPERATION

Using 15 pulses per half-cycle and a filter break frequency of 1100 Hz, an output sinewave of about 1% total harmonic distortion and less than 1% ripple was achieved.

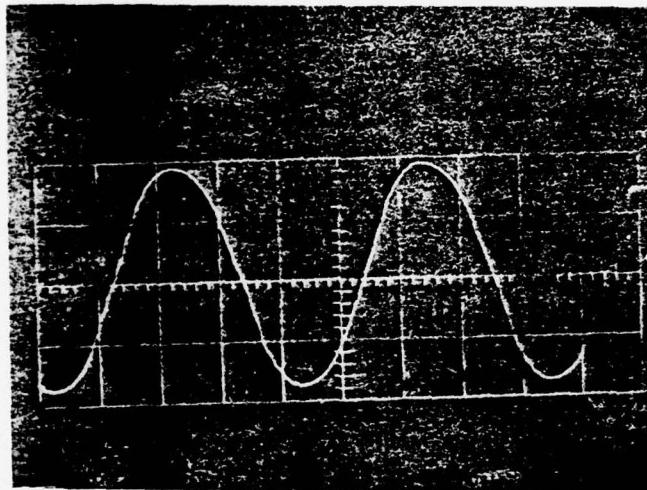


Figure 3.2.7.7-2 400Hz sinewave into 2 ohm load
using 1st method of PWM

3.2.7.8 RESULTS

The following pictures further document the results of the work efforts performed using the 1st type of PWM. This type of modulation is where only one switch is on per half-cycle. The impedance is high during its off time.

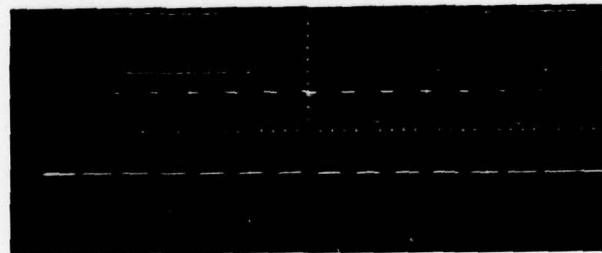


Figure 3.2.7.8-1 Ideal sinusoidal distribution, no bias, no rotation, with approximately 512 of the 2048 total bits on (that is, the sum of the on times for all the pulses of the half-cycle is about 25% of the total).

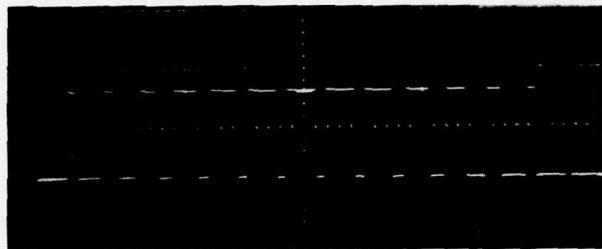


Figure 3.2.7.8-2 The same as above, but with about a 50% (1024 bits on) duty cycle. Note that an odd number of pulses places a pulse in the middle of the half-cycle.

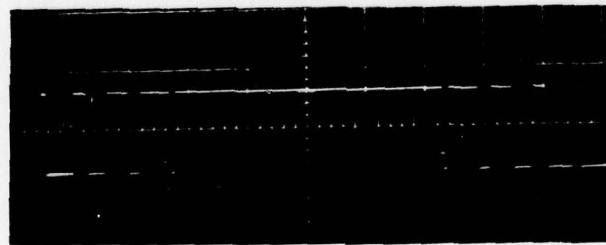


Figure 3.2.7.8-3 The same as above, except that the duty cycle is about 75%. The intervals near the center of the pulse sequence are totally on.

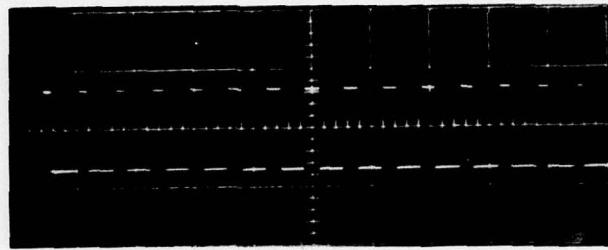


Figure 3.2.7.8-4 Biased pulse sequence. The width of the center pulse is the same as in Figure 1a, but the pulses on each side of the center pulse are wider. The pulses still decrease sinusoidally in width from the center of the outside.

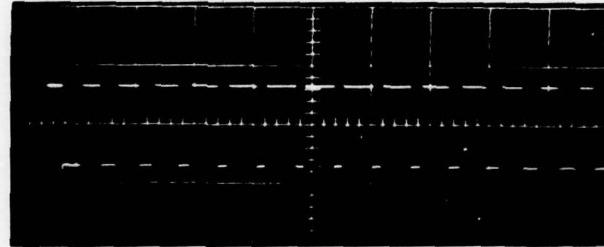


Figure 3.2.7.8-5 Biased pulse sequence. The center pulse is the same width as in Figure 1b. This type of pulse sequence currently produces the lowest distortion sinewave at the output of the filter when operating at 400 Hz. The power factor of Figure 2b is \$480 (56%).

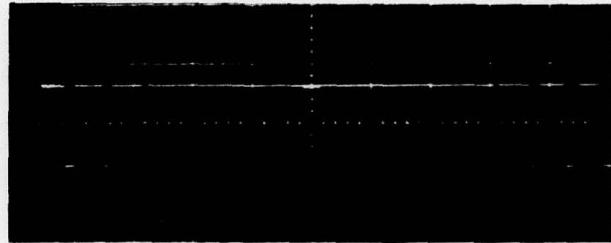


Figure 3.2.7.8-6 Biased pulse sequence. Based on Fibure lc, the total on time in the center is greater than in lc. This type of pulse sequence could be used to deliver a large amount of power to the load in a short period of time.

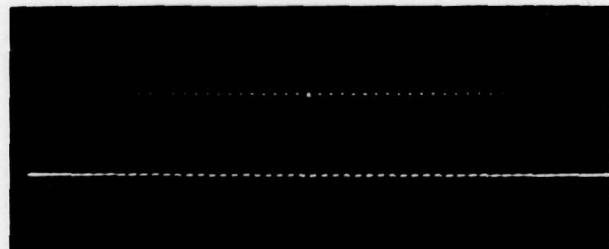


Figure 3.2.7.8-7 Ideal sinusoidal distribution, no bias, no rotation, with about 512 of 2048 bits on (25% duty cycles), with 51 pulses.

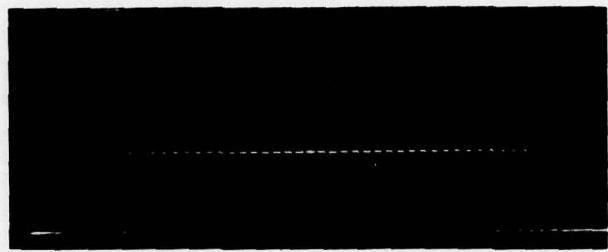


Figure 3.2.7.8-8 Same as above, with a 50% duty cycle.



Figure 3.2.7.8-9 Same as above, with about a 75% duty cycle.

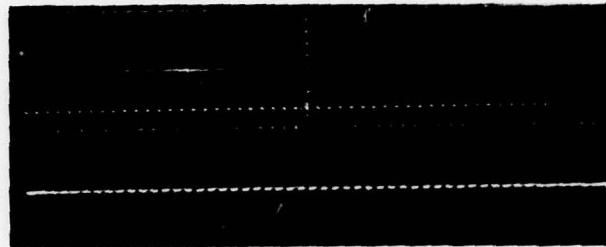


Figure 3.2.7.8-10 Biased pulse sequence. The pulses look nearly equal but are really decreasing from the center to the outside (CRT astigmatism and focus where not uniform across the CRT face).

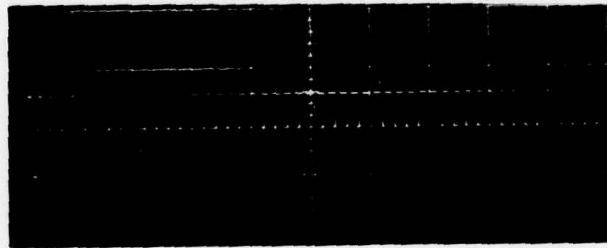


Figure 3.2.7.8-11 Biased pulse sequence. Power factor of \$400 (50%). At Hz operation, the lowest ripple and distortion was achieved with a power factor of \$500 (63%). The wider pulses on the outsides are apparently compensating for switching and filter losses.

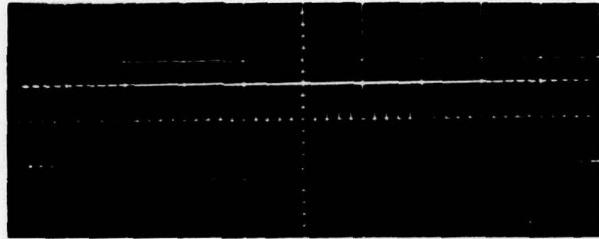


Figure 3.2.7.8-12 Biased pulse sequence. Duty cycle at 75%.

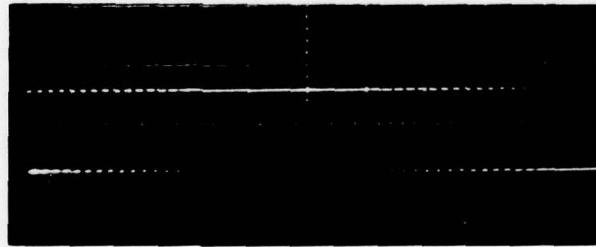


Figure 3.2.7.8-13 A demonstration of the rotation capability of the software. Notice that the center region of the pulse sequence (as in Figure 3b) is to the left of center in the above photo. This allows a distortion due to lag in the filter to be removed, and may allow phase shift control, with leading and lagging loads.

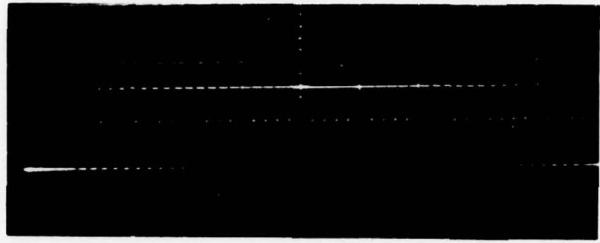


Figure 3.2.7.8-14 The same as above, except that the rotation is to the right of center. Any degree of rotation can be achieved, with 1 bit in 2048 resolution.



Figure 3.2.7.8-15 A frequency spectrum of 51 pulses per half-cycle pulse sequence (unfiltered). At 50 Hz (102 pulses per cycle), the harmonic peak at 5.1K Hz., 10.2K Hz., 15.3K Hz., etc. The output filter (break frequency = 180 Hz.). Attenuates these high order harmonics by about 50 db.

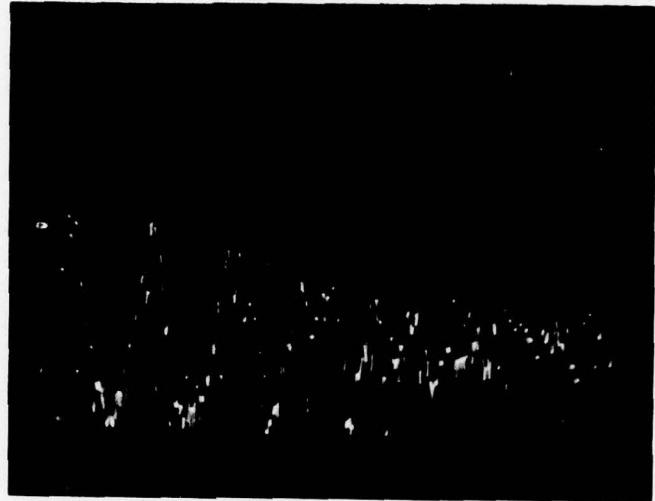


Figure 3.2.7.8-16 A frequency spectrum of 15 pulses per half-cycle pulse sequence (unfiltered). At 400 Hz. (30 pulses per cycle), the harmonics peak at 12KHz., 24Khz., 36Khz., etc. The output filter (break frequency at 1100 Hz.) attenuates these harmonics by at least 50 db.

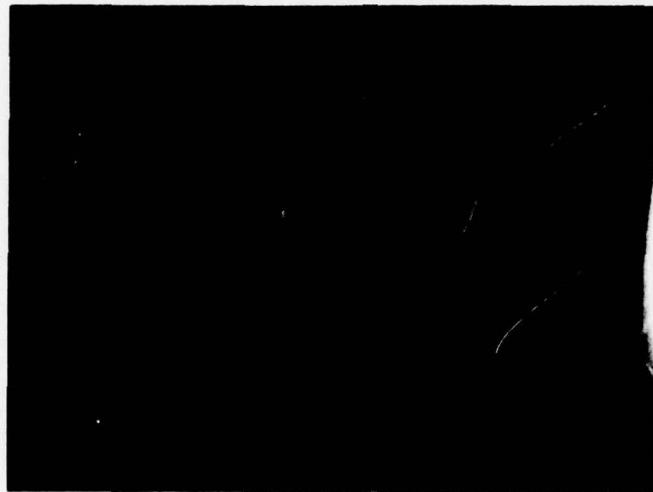


Figure 3.2.7.8-17 Three phase 60 Hz full load.

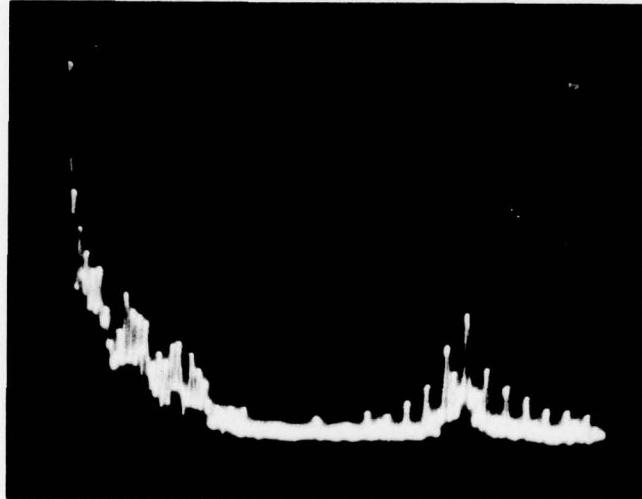


Figure 3.2.7.8-18 Frequency spectrum 60 Hz full load.
Less than 1% distortion.

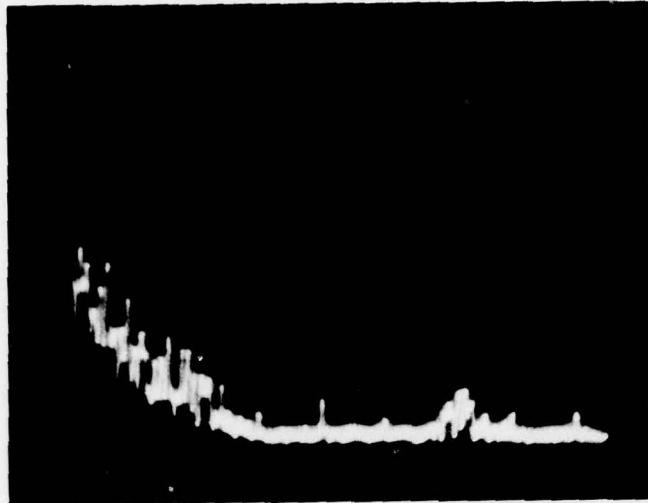


Figure 3.2.7.8-19 Frequency spectrum line to line.

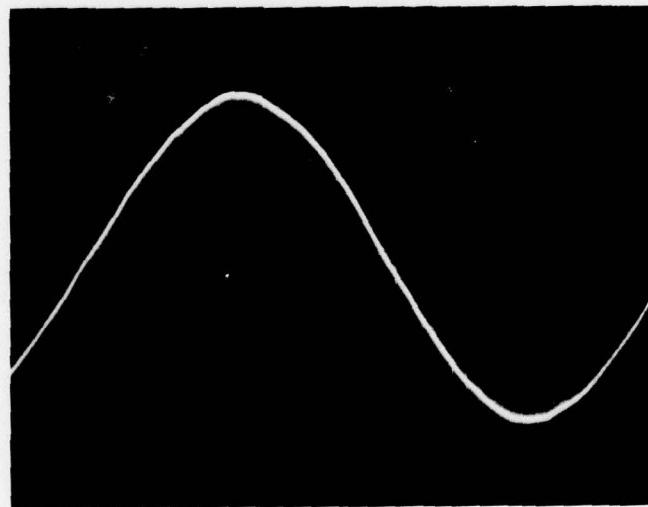


Figure 3.2.7.8-20 Output voltage line to line.

3.2.7.9 INSTRUCTION FOR AND ASSEMBLY LISTINGS

3.2.7.9.1 INSTRUCTION ON USE

For the main driver program, the program is properly activated by entering the program at location 2147 (Hexidecimal). This will initialize the system to a pulse number based upon switch setting for either 50, 50, or 400 Hz. The processor also automatically initializes itself to the proper phase relations for single phase 120, single phase 120 and three phase 120.

00001 NAM INVERTER PROGRAM (3 PHASE/FEEDBACK).
00002 OPT D=OBJECT
00003 ◆
00004 ◆
00005 2000 ORG \$2000 ROM STARTS AT \$2000.
00006 ◆
00007 ◆
00008 ◆ AUG. 30, 1976
00009 ◆
00010 ◆
00011 ◆ THIS PROGRAM GENERATES SINUSOIDALLY MODULATED
00012 ◆ PULSE SEQUENCES (3 PHASED) TO DRIVE 3 INTEGRATED
00013 ◆ POWER SWITCHES. THE OUTPUTS OF THE POWER SWITCHES
00014 ◆ ARE FILTERED TO PRODUCE A SINE WAVE OF 50, 60 OR
00015 ◆ 400 HZ.
00016 ◆
00017 ◆ THE INVERTER SYSTEM INCLUDES A HIGH VOLTAGE
00018 ◆ AND CURRENT POWER SUPPLY AND VARIOUS LOGIC SUPPLIES
00019 ◆ A MICROPROCESSOR AND MEMORY SYSTEM, AN A TO D
00020 ◆ CONVERTER WITH SAMPLE-AND-HOLDS AND ANALOG
00021 ◆ MULTIPLEXOR, 3 INTEGRATED POWER SWITCHES WITH
00022 ◆ ASSOCIATED PROTECTIVE CIRCUITRY, AND THE FILTER
00023 ◆ SECTION. THIS PROGRAM PROVIDES A PULSE SEQUENCE
00024 ◆ TO DRIVE THE POWER SWITCHES VIA A BUFFERED RANDOM
00025 ◆ ACCESS MEMORY.
00026 ◆
00027 ◆ THE OBJECT OF THIS PROGRAM IS TO PROVIDE THE
00028 ◆ BEST SET OF PULSES POSSIBLE TO KEEP THE OUTPUT
00029 ◆ AMPLITUDE WITHIN SPECIFICATIONS. THE FREQUENCY
00030 ◆ OF THE OUTPUT IS REFERENCED TO A STABLE CLOCK
00031 ◆ AND THE HARMONIC CONTENT OF THE OUTPUT SIGNAL IS
00032 ◆ DETERMINED BY THE NUMBER OF PULSES PER HALF-CYCLE
00033 ◆ AND THE FILTER CONFIGURATION. THE MAIN TASK OF
00034 ◆ THE FEEDBACK CIRCUITRY AND PROGRAM IS MINIMIZED
00035 ◆ TO KEEPING THE OUTPUT AMPLITUDE AS CLOSE TO
00036 ◆ 120V RMS AS POSSIBLE FOR ALL LOADS FROM .8 LAGGING
00037 ◆ TO .8 LEADING AT CURRENT LEVELS UP TO 41A RMS.
00038 ◆ AT FREQUENCIES OF 50, 60, AND 400 HZ.
00039 ◆

00041 ◆ THE FOLLOWING TABLE CONTAINS THE DATA REQUIRED
 00042 ◆ TO GENERATE 9, 61, AND 71 PULSES/HALF-CYCLE. EACH
 00043 ◆ NUMBER REPRESENTS THE PERCENTAGE OF THE TOTAL
 00044 ◆ ON TIME PER HALF-CYCLE FOR A SPECIFIC PULSE,
 00045 ◆ INDEPENDENT OF THE DUTY CYCLE AND FREQUENCY. THE
 00046 ◆ CENTER PULSE IS BIASED TO 65535 AND THE VALUES
 00047 ◆ FOR THE OTHER PULSES ARE DETERMINED BY THEIR SIZE
 00048 ◆ RELATIVE TO THE CENTER PULSE.
 00049 ◆
 00050 ◆ 9 PULSES (400 HZ OPERATION).
 00051 ◆
 00052 2000 2C74 STAB9 FDB 11380,32768,50203,61583
 2002 8000
 2004 C41B
 2006 F08F
 00053 ◆
 00054 ◆ 61 PULSES (60 HZ OPERATION).
 00055 ◆
 00056 2008 0697 STAB61 FDB 1687,5057,8414,11749,15053
 200A 13C1
 200C 20DE
 200E 2DE5
 2010 3ACD
 00057 2012 478C FDB 18316,21531,24688,27781,30799
 2014 541B
 2016 6070
 2018 6085
 201A 794F
 00058 201C 83C8 FDB 33736,36584,39335,41981,44516
 201E 8EE9
 2020 99A7
 2022 A3FD
 2024 ADE4
 00059 2026 B755 FDB 46933,49225,51387,53412,55296
 2028 C049
 202A C888
 202C D0A4
 202E D800
 00060 2030 DECA FDB 57034,58620,60050,61322,62430
 2032 E4FC
 2034 EA92
 2036 EF3A
 2038 F3DE
 00061 203A F78E FDB 63374,64149,64754,65187,65448
 203C FA95
 203E FCF2
 2040 FEA3
 2042 FFA8
 00062 ◆
 00063 ◆ 71 PULSES (50 HZ OPERATION).
 00064 ◆
 00065 2044 05A9 STAB71 FDB 1449,4346,7234,10108,12962
 2046 10FA
 2048 1C42

	2048 277C	
	204C 3282	
00066	204E 3D9F	FDB 15791,18589,21351,24071,26743
	2050 439D	
	2052 5367	
	2054 5E07	
	2056 6877	
00067	2058 72B4	FDB 29364,31926,34427,36860,39220
	205A 7CB6	
	205C 867B	
	205E 8FFC	
	2060 9934	
00068	2062 A220	FDB 41504,43707,45824,47852,49786
	2064 ABBB	
	2066 B300	
	2068 BAEC	
	206A C27A	
00069	206C C986	FDB 51622,53357,54988,56511,57924
	206E D06D	
	2070 D6CC	
	2072 DCBF	
	2074 E244	
00070	2076 E757	FDB 59223,60406,61471,62416,63238
	2078 EBF6	
	207A F01F	
	207C F3D0	
	207E F706	
00071	2080 F9C1	FDB 63937,64511,64958,65278,65470
	2082 FBFF	
	2084 FD8E	
	2086 FEFE	
	2088 FF8E	

PHASE 004 INVERTER

00073		♦		
00074		♦	EQUIVALENCES AND RESERVED MEMORY.	
00075		♦		
00076	4000	PIA1RD EQU	\$4000	R/D INPUT REGISTER.
00077	4001	PIA1RC EQU	\$4001	CONTROL REGISTER.
00078	4002	PIA1BD EQU	\$4002	MUX, BUFFER, AND FREQ. SELECT
00079	4003	PIA1BC EQU	\$4003	CONTROL REGISTER.
00080		♦		
00081	2038 0024	ONTAB RMB	36	ON TABLE STORAGE.
00082	208E 0024	OFFTAB RMB	36	OFF TABLE STORAGE.
00083		♦		
00084	2002 0002	ON RMB	2	ON TABLE POINTER.
00085	2004 0002	OFF RMB	2	OFF TABLE POINTER.
00086		♦		
00087	20D6 0002	SNPSHT RMB	2	TOP OF SNAPSHOT STORAGE.
00088	20D8 0001	COUNTR RMB	1	SNAPSHOT ENTRY COUNTER.
00089		♦		
00090	20D9 0002	TEMP RMB	2	TEMPORARY POWER FACTOR STORAGE
00091	20DE 0002	TIME RMB	2	TIME DELAY PARAMETER.
00092		♦		
00093	20DD 0001	N RMB	1	PULSES PER HALF-CYCLE.
00094		♦		
00095	20DE 0002	PFFACT RMB	2	CONVERTED POWER FACTOR.
00096		♦		
00097	20E0 0002	SINADR RMB	2	SINE TABLE POINTER.
00098		♦		
00099	20E2 0001	INTVL RMB	1	BITS PER PULSE INTERVAL.
00100	20E3 0001	HALFIN RMB	1	1/2 BITS PER PULSE INTERVAL.
00101		♦		
00102	20E4 0002	ROTATE RMB	2	PULSE PROGRAM LOAD OFFSET.
00103	20E6 0002	ROTAT1 RMB	2	PHASE 1 OFFSET.
00104	20E8 0002	ROTAT2 RMB	2	PHASE 2 OFFSET.
00105	20EA 0003	ROTAT3 RMB	3	PHASE 3 OFFSET.
00106		♦		
00107	20ED 0002	POWER RMB	2	PULSE PROGRAM POWER PARAMETER
00108	20EF 0002	POWER1 RMB	2	PHASE 1 POWER FACTOR.
00109	20F1 0002	POWER2 RMB	2	PHASE 2 POWER FACTOR.
00110	20F3 0002	POWER3 RMB	2	PHASE 3 POWER FACTOR.
00111		♦		
00112	20F5 0002	MINPR RMB	2	MAX AND MIN POWER KEEP PULSE
00113	20F7 0002	MAXPR RMB	2	WIDTHS WITHIN KNOWN LIMITS.
00114		♦		
00115	20F9 0001	DELTA RMB	1	FEEDBACK CONTROL INCREMENT.
00116		♦		
00117	20FA 0002	PULSNM RMB	2	PULSE NUMBER (MUST BE 2 BYTES)
00118		♦		
00119	20FC 0002	ACTUAL RMB	2	PULSE ERROR CORRECTION.
00120		♦		
00121	20FE 0002	PULSX RMB	2	PULSE ADDRESS.
00122		♦		
00123	2100 0002	TOTAL RMB	2	BITS/CYCLE.
00124	2102 0002	HAFTOT RMB	2	BITS/HALF-CYCLE.

00126	◆	PROGRAM DATA (FOR 50, 60, & 400 HZ.)		
00127	◆			
00128 2104 0400	TIME50 FDB	\$400	50 HZ TIME DELAY.	
00129 2106 0400	TIME60 FDB	\$400	60 HZ TIME DELAY.	
00130 2108 0400	TIM400 FDB	\$400	400 Hz TIME DELAY.	
00131	◆			
00132 210A 2000	SINE9 FDB	\$2000	9 PULSES/HALFCYCLE DATA ADDR.	
00133 210C 2000	SINE61 FDB	\$2008	61 PULSES/HALFCYCLE DATA ADDR	
00134 210E 2044	SINE71 FDB	\$2044	71 PULSES/HALFCYCLE DATA ADDR	
00135	◆			
00136 2110 E3	INTV9 FCB	227	BITS/INTVL FOR 9 PULSES.	
00137 2111 43	INTV61 FCB	67	BITS/INTVL FOR 61 PULSES.	
00138 2112 39	INTV71 FCB	57	BITS/INTVL FOR 71 PULSES.	
00139	◆			
00140 2113 71	HALF9 FCB	113	BITS/HALF-INTVL FOR 9 PULSES.	
00141 2114 e1	HALF61 FCB	33	BITS/HALF-INTVL FOR 61 PULSES.	
00142 2115 10	HALF71 FCB	28	BITS/HALF-INTVL FOR 71 PULSES	
00143	◆			
00144 2116 0FFF	ROT4K1 FDB	\$FFF	PHASE 1 ROTATION, 50-60 Hz.	
00145 2118 0849	ROT4K2 FDB	\$8A9	PHASE 2 ROTATION, 50-60 Hz.	
00146 211A 0554	ROT4K3 FDB	\$554	PHASE 3 ROTATION, 50-60 Hz.	
00147	◆			
00148 211C 07FF	ROT2K1 FDB	\$7FF	PHASE 1 ROTATION, 400 Hz.	
00149 211E 0554	ROT2K2 FDB	\$554	PHASE 2 ROTATION, 400 Hz.	
00150 2120 02A8	ROT2K3 FDB	\$2A8	PHASE 3 ROTATION, 400 Hz.	
00151	◆			
00152 2122 0100	PWR2K FDB	\$100	INITIAL POWER FACTOR FOR 400	
00153 2124 0200	PWR4K FDB	\$300	INIT. P. F. FOR 50-60 Hz.	
00154	◆			
00155 2126 00	CNTMIN FCB	\$00	MINIMUM H/D VALUE DESIRED.	
00156 2127 60	CNTMAX FCB	\$60	MAXIMUM H/D VALUE DESIRED.	
00157	◆			
00158 2128 0300	MNP50 FDB	\$300	50 Hz MINIMUM POWER FACTOR.	
00159 2128 0400	MXP50 FDB	\$400	50 Hz MAXIMUM POWER FACTOR.	
00160	◆			
00161 212C 0300	MNP60 FDB	\$300	60 Hz MINIMUM POWER FACTOR.	
00162 212E 0400	MXP60 FDB	\$400	60 Hz MAXIMUM POWER FACTOR.	
00163	◆			
00164 2130 0100	MNP400 FDB	\$100	400 Hz MINIMUM POWER FACTOR.	
00165 2132 01E0	MXP400 FDB	\$1E0	400 Hz MAXIMUM POWER FACTOR.	
00166	◆			
00167 2134 04	DLT50 FCB	\$4	50 Hz FEEDBACK INCREMENT.	
00168 2136 04	DLT60 FCB	\$4	60 Hz FEEDBACK INCREMENT.	
00169 2136 04	DLT400 FCB	\$4	400 Hz FEEDBACK INCREMENT.	
00170	◆			
00171 2137 0008	PULS9 FDB	9	9 PULSES/HALF-CYCLE (400 Hz).	
00172 2139 0020	PULS61 FDB	61	61 PULSES/HALF-CYCLE (60 Hz).	
00173 213B 0047	PULS71 FDB	71	71 PULSES/HALF-CYCLE (50 Hz).	
00174	◆			
00175 2140 0300	TOT2K FDB	\$800	BITS/CYCLE, (400 Hz.)	
00176 213F 1000	TOT4K FDB	\$1000	BITS/CYCLE, (50-60 Hz.)	
00177 2141 H400	PRBIAS FDB	41984	POWER BIAS FACTOR.	
00178 2143 0400	HALF2K FDB	\$400	BITS/HALF-CYCLE, (400 Hz.)	
00179 2145 0800	HALF4K FDB	\$800	BITS/HALF-CYCLE, (50-60 Hz.)	

00181	◆	EXECUTION BEGINS HERE.		
00182	◆	INITIALIZE THE PIA AND STACK POINTER.		
00183	◆			
00184 2147 8E 2700	INITL LDS	#\$2700	LOAD THE STACK POINTER.	
00185	◆			
00186 214B 7F 4001	CLR	PIA1AC	SELECT DATA DIRECTION REG'S.	
00187 214D 7F 4003	CLR	PIA1BC		
00188 2150 7F 4000	CLR	PIA1AD	SET THE A-SIDE TO INPUTS.	
00189 2153 86 07	LDA A	#\$7		
00190 2155 B7 4002	STA A	PIA1BD	SET BITS 0-2 AS OUTPUTS, BITS 3-7 AS INPUTS.	
00191	◆	SELECT PERIPHERAL REGISTERS.		
00192 2158 C6 04	LDA B	#\$4		
00193 215A F7 4001	STA B	PIA1AC		
00194 215D F7 4003	STA B	PIA1BC		
00195 2160 C6 36	LDA B	#\$36	SET CA2 LOW, ENABLE CA1 AS AN INTERRUPT INPUT, ACTIVE ON A POSITIVE TRANSITION.	
00196 2162 F7 4001	STA B	PIA1AD		
00197	◆			
00198	◆			
00199 2165 CE 37FF	LDX	#\$37FF	INITIALIZE SNAPSHOT ROUTINE.	
00200 2168 FF 20D6	STX	SNPSHT	TOP OF SNAPSHOT RECORD AREA.	
00201 216B 86 FF	LDA A	#\$FF	128 SNAPSHOTS ARE TAKEN.	
00202 216D B7 20D8	STA A	COUNTP		
00203	◆			
00204	◆	50, 60, AND 400 HZ INITIALIZATION. BITS 3, 4,		
00205	◆	AND 5 ARE FOR 50, 60, AND 400 HZ, RESPECTIVELY.		
00206	◆			
00207 2170 C6 20	LDA B	#\$20	CHECK THE FREQUENCY SWITCH.	
00208 2172 F5 4002	BIT B	PIA1BD	IS BIT 5 (400 HZ) SET?	
00209 2175 27 03	BEO	NOT400	IF SO, SET 400 HZ PARAMETERS.	
00210 2177 7E 220F	JMP	FIX400		
00211	◆			
00212 217A FE 2124	NOT400 LDX	PWR4K	INITIAL POWER FACTOR FOR	
00213 217D FF 20EF	STX	POWER1	50/60 HZ.	
00214 2180 FF 20F1	STX	POWER2		
00215 2183 FF 20F3	STX	POWER3		
00216	◆			
00217 2186 FE 2116	LDX	ROT4K1	SET-UP 50/60 HZ ROTATION	
00218 2189 FF 20E6	STX	ROTAT1	FOR LOADING THE 3 DRIVER RAMS.	
00219	◆			
00220 218C FE 213F	LDX	TOT4K	BITS/CYCLE.	
00221 218F FF 2100	STX	TOTAL		
00222	◆			
00223 2192 FE 2145	LDX	HALF4K	BITS/HALF-CYCLE.	
00224 2195 FF 2102	STX	HAFTOT		
00225	◆			
00226 2198 FE 2118	LDX	ROT4K2		
00227 219B FF 20E8	STX	ROTAT2		
00228	◆			
00229 219E FE 211A	LDX	ROT4K3		
00230 21A1 FF 20EA	STX	ROTAT3		
00231	◆			
00232 21A4 57	ASR B			
00233 21A5 F5 4002	BIT B	PIA1BD	IS BIT 4 (60 HZ) SET?	
00234 21A8 26 33	BNE	FIX60	IF SO, SET 60 HZ PARAMETERS.	

00236	21AA FE 213B	FIX50	LDX	PULS71	INITIALIZE 50 HZ PULSE NUMBER
00237	21AD FF 20FA		STX	PULSNM	
00238	◆				
00239	21B0 B6 2112		LDA A	INTV71	INITIALIZE BITS/INTVL FOR
00240	21B3 B7 20E2		STA A	INTVL	50 HZ.
00241	◆				
00242	21B6 B6 2115		LDA A	HALF71	INITIALIZE BITS/HALF INTV
00243	21B9 B7 20E3		STA A	HALFIN	FOR 50 HZ.
00244	◆				
00245	21BC B6 2134		LDA A	DLT50	SET 50 HZ FEEDBACK DELTA.
00246	21BF B7 20F9		STA A	DELTA	
00247	◆				
00248	21C2 FE 2104		LDX	TIME50	SET 50 HZ TIME DELAY.
00249	21C5 FF 20DB		STX	TIME	
00250	◆				
00251	21C8 FE 210E		LDX	SINE71	SET 50 HZ SINE TABLE ADDRESS.
00252	21CB FF 20E0		STX	SINADR	
00253	◆				
00254	21CE FE 2128		LDX	MNP50	SET MINIMUM POWER FOR 50 HZ.
00255	21D1 FF 20F5		STX	MINPR	
00256	◆				
00257	21D4 FE 212A		LDX	MXP50	SET MAXIMUM POWER FOR 50 HZ.
00258	21D7 FF 20F7		STX	MAXPR	
00259	◆				
00260	21DA 7E 2269		JMP	PHASE1	GENERATE 50 HZ PULSE SEQUENCE
00261	◆				
00262	◆				
00263	21DD FE 2139	FIX60	LDX	PULS61	SET 60 HZ PULSE NUMBER.
00264	21E0 FF 20FA		STX	PULSNM	
00265	◆				
00266	21E3 B6 2111		LDA A	INTV61	SET BITS/INTVL FOR 60 HZ.
00267	21E6 B7 20E2		STA A	INTVL	
00268	◆				
00269	21E9 B6 2114		LDA A	HALF61	SET BITS/HALF-INTV FOR 60 HZ.
00270	21EC B7 20E3		STA A	HALFIN	
00271	◆				
00272	21EF B6 2135		LDA A	DLT60	SET FEEDBACK DELTA FOR 60 HZ.
00273	21F2 B7 20F9		STA A	DELTA	
00274	◆				
00275	21F5 FE 2106		LDX	TIME60	SET 60 HZ TIME DELAY.
00276	21F8 FF 20DB		STX	TIME	
00277	◆				
00278	21FB FE 210C		LDX	SINE61	SET 60 HZ SINE TABLE ADDRESS.
00279	21FE FF 20E0		STX	SINADR	
00280	◆				
00281	2201 FE 2120		LDX	MNP60	SET 60 HZ MINIMUM POWER FACTO
00282	2204 FF 20F5		STX	MINPR	
00283	◆				
00284	2207 FE 212E		LDX	MXP60	SET 60 HZ MAXIMUM POWER FACTO
00285	220A FF 20F7		STX	MAXPR	
00286	◆				
00287	220D 20 5A		BRA	PHASE1	GENERATE 60 HZ PULSE SEQUENCE

00289	♦				
00290	220F FE 2137	FIX400	LDX	PULS9	SET PULSE NUMBER TO 9 FOR
00291	2212 FF 20FA		STX	PULSNM	400 HZ.
00292	♦				
00293	2215 B6 2110		LDA A	INTV9	SET BITS/INTVL FOR 400 HZ.
00294	2218 B7 20E2		STA A	INTVL	
00295	♦				
00296	221B B6 2113		LDA A	HALF9	SET BITS/HALF-INTV FOR 400 HZ
00297	221E B7 20E3		STA A	HALFIN	
00298	♦				
00299	2221 B6 2136		LDA A	DLT400	SET FEEDBACK DELTA FOR 400 HZ
00300	2224 B7 20F9		STA A	DELTA	
00301	♦				
00302	2227 FE 211C		LDX	ROT2K1	SET 2K ROTATION FOR PHASE 1.
00303	222A FF 20E6		STX	ROTAT1	
00304	♦				
00305	222D FE 213D		LDX	TOT2K	BITS/CYCLE.
00306	2230 FF 2100		STX	TOTAL	
00307	♦				
00308	2233 FE 2143		LDX	HALF2K	BITS/HALF-CYCLE.
00309	2236 FF 2102		STX	HAFTOT	
00310	♦				
00311	2239 FE 211E		LDX	ROT2K2	SET 2K ROTATION FOR PHASE 2.
00312	223C FF 20E8		STX	ROTAT2	-
00313	♦				
00314	223F FE 2120		LDX	ROT2K3	SET 2K ROTATION FOR PHASE 3.
00315	2242 FF 20EA		STX	ROTAT3	
00316	♦				
00317	2245 FE 2122		LDX	PWR2K	SET 400 HZ POWER FACTORS.
00318	2248 FF 20EF		STX	POWER1	
00319	224B FF 20F1		STX	POWER2	
00320	224E FF 20F3		STX	POWER3	
00321	♦				
00322	2251 FE 2108		LDX	TIM400	SET 400 HZ TIME DELAY.
00323	2254 FF 20DB		STX	TIME	
00324	♦				
00325	2257 FE 210A		LDX	SINE9	SET 400 HZ SINE TABLE ADDRESS
00326	225A FF 20E0		STX	SINADR	
00327	♦				
00328	225D FE 2130		LDX	MNP400	SET 400 HZ MIN POWER FACTOR.
00329	2260 FF 20F5		STX	MINPP	
00330	♦				
00331	2263 FE 2132		LDX	MXP400	SET 400 HZ MAX POWER FACTOR.
00332	2266 FF 20F7		STX	MAXPP	

00334	♦			
00335	♦	EXECUTIVE ROUTINE.	SEQUENTIAL PHASE UPDATE.	
00336	♦			
00337 2269 5F	PHASE1 CLR B			SELECT PHASE 1, MUX 1.
00338 226A FE 20EF	LDX	POWER1		GET PHASE 1 POWER FACTOR.
00339 226D FF 20D9	STX	TEMP		SAVE TEMPORARILY.
00340 2270 FE 20E6	LDX	ROTAT1		GET PHASE 1 ROTATION.
00341 2273 8D 2E	BSR	FEEDBK		CHECK PHASE 1 A/D VALUE.
00342	♦			
00343 2275 FE 20ED	LDX	POWER		GET UPDATED POWER FACTOR.
00344 2278 FF 20EF	STX	POWER1		SAVE FOR NEXT PHASE 1 UPDATE.
00345	♦			
00346 227B C6 01	PHASE2 LDA B	#\$1		SELECT PHASE 2, MUX 2.
00347 227D FE 20F1	LDX	POWER2		GET PHASE 2 POWER FACTOR.
00348 2280 FF 20D9	STX	TEMP		SAVE TEMPORARILY.
00349 2283 FE 20E8	LDX	ROTAT2		GET PHASE 2 ROTATION.
00350 2286 8D 1B	BSR	FEEDBK		CHECK PHASE 2 A/D VALUE.
00351	♦			
00352 2288 FE 20ED	LDX	POWER		GET UPDATED POWER FACTOR.
00353 228B FF 20F1	STX	POWER2		SAVE FOR NEXT PHASE 2 UPDATE.
00354	♦			
00355 228E C6 02	PHASE3 LDA B	#\$2		SELECT PHASE 3, MUX 3.
00356 2290 FE 20F3	LDX	POWER3		GET PHASE 3 POWER FACTOR.
00357 2293 FF 20D9	STX	TEMP		SAVE TEMPORARILY.
00358 2296 FE 20EA	LDX	ROTAT3		GET PHASE 3 ROTATION.
00359 2299 8D 08	BSR	FEEDBK		CHECK PHASE 3 A/D VALUE.
00360	♦			
00361 229B FE 20ED	LDX	POWER		GET UPDATED POWER FACTOR.
00362 229E FF 20F3	STX	POWER3		SAVE FOR NEXT PHASE 3 UPDATE.
00363	♦			
00364 22A1 20 C6	BRA	PHASE1		CYCLE THRU PHASES AGAIN.

00366	◆			
00367	◆	FEEDBK	LDA A #\$FC	SELECT A PHASE BUFFER AND MUX
00368	◆		AND A PIA1BD	
00369 22A3	86 FC	FEEDBK	LDA A #\$FC	SELECT A PHASE BUFFER AND MUX
00370 22A5	B4 4002		AND A PIA1BD	
00371 22A8	1B		ABA	
00372 22A9	B7 4002		STA A PIA1BD	
00373	◆			
00374 22AC	FF 20E4		STX ROTATE	SET ROTATION FOR PHASE OFFSET
00375	◆			
00376 22AF	B6 4000	CONVRT	LDA A PIA1AD	CLEAR THE INTERRUPT FLAG BIT.
00377	◆			
00378 22B2	86 3E		LDA A #\$3E	A POSITIVE TRANSITION ON
00379 22B4	B7 4001		STA A PIA1AC	CA2 STARTS THE A/D CONVERSION
00380 22B7	86 36		LDA A #\$36	RESET CA2.
00381 22B9	B7 4001		STA A PIA1AC	
00382	◆			
00383 22BC	B6 4001	EDC	LDA A PIA1AC	WAIT FOR END OF CONVERSION.
00384 22BF	2A FB		BPL EDC	CA1 IS USED FOR EDC INPUT.
00385	◆			
00386	◆	SNAPSHOT	ROUTINE.	
00387	◆			
00388 22C1	FE 20D6		LDX SNPSHT	SNAPSHOT MEMORY POINTER.
00389	◆			
00390 22C4	B6 20D9		LDA A TEMP	OBTAIN THE POWER FACTOR FOR
00391 22C7	36		PSH A	SAVE A TEMPORARILY.
00392 22C8	F6 20DA		LDA B TEMP+1	THE PHASE BEING UPDATED.
00393 22CB	A7 00		STA A 0,X	STORE THE CURRENT POWER
00394 22CD	09		DEX	FACTOR IN SNAPSHOT MEMORY.
00395 22CE	E7 00		STA B 0,X	(BOTH BYTES).
00396 22D0	09		DEX	
00397	◆			
00398 22D1	B6 4000		LDA A PIA1AD	GET THE A/D VALUE.
00399 22D4	A7 00		STA A 0,X	STORE IT IN SNAPSHOT MEMORY.
00400 22D6	03		DEX	DECREMENT MEMORY POINTER.
00401	◆			
00402 22D7	FF 20D6		STX SNPSHT	SAVE SNAPSHOT POINTER.
00403 22DA	7A 20D8		DEC COUNTR	COUNT THE SNAPSHOT ENTRY.
00404	◆			
00405 22DD	27 42		BEQ STOP	SWI IF SNAPSHOT IS FINISHED.

00407	◆	FEEDBACK ALGORITHM (16 BIT VERSION).			
00408	◆	IS A/D VALUE > CNTVL VALUE?			
00409	◆	IF >, DECREMENT POWER FACTOR.			
00410 22DF B1 2127	UPDATE CMP A	CNTMAX			
00411 22E2 22 19	BHI	DECRMT			
00412	◆				
00413 22E4 B1 2126	CMP A	CNTMIN	A/D > CONTROL MINIMUM?		
00414 22E7 22 36	BHI	RETN1	IF SO, A/D WITHIN DEADBAND.		
00415	◆				
00416 22E9 32	INCRMT	PUL A	RESTORE A REG.		
00417 22EA B1 20F7	CMP A	MAXPR	IS POWER ALREADY > MAXPR?		
00418 22ED 22 31	BHI	RETURN	TEST MSB OF PWR VS. MAXPR MSB		
00419 22EF 26 05	BNE	PWRUP			
00420 22F1 F1 20F8	CMP B	MAXPR+1			
00421 22F4 22 2A	BHI	RETURN			
00422 22F6 FB 20F9	PWRUP	ADD B	DELTA	TEST LSB OF PWR VS. MAXPR LSB	
00423 22F9 89 00	ADC A	#\$0	ADD VARIABLE POWER INCREMENT.		
00424 22FB 20 12	BRA	FIXPR	POWER FACTOR INCREASED.		
00425	◆				
00426 22FD 32	DECRMT	PUL A	RESTORE A REG.		
00427 22FE B1 20F5	CMP A	MINPR	IS POWER ALREADY < MINPR.		
00428 2301 2D 10	BLT	RETURN	PWR VALUE MSB < MINPR MSB?		
00429 2303 26 05	BNE	PWRDOWN			
00430 2305 F1 20F6	CMP B	MINPR+1			
00431 2308 2D 16	BLT	RETURN			
00432 230A F0 20F9	PWRDOWN	SUB B	DELTA	PWR VALUE LSB < MINPR LSB?	
00433 230D 22 00	SBC A	#\$0	SUB VARIABLE POWER INCREMENT.		
00434	◆				
00435 230F B7 20ED	FIXPR	STA A	POWER	UPDATE PULSE PROGRAM POWER	
00436 2312 F7 20EE		STA B	POWER+1	FACTOR.	
00437	◆				
00438 2315 8D 08		BSR	PULSE	CALCULATE NEW PULSE SEQUENCE.	
00439	◆				
00440 2317 FE 200B		LDX	TIME	TIME IS THE DELAY VARIABLE.	
00441 231A 09	DELAY	DEX			
00442 231B 26 FD		BNE	DELAY		
00443	◆				
00444 231D 20 01		BRA	RETURN		
00445 231F 32	RETN1	PUL A		ADJUST STACK.	
00446 2320 39	RETURN	RTS		RETURN TO EXEC SCAN LOOP.	
00447	◆				
00448 2321 3F	STOP	SMI	INTERRUPT IN SNAPSHOT IS FULL.		

00450 ♦
00451 ♦
00452 ♦ CALCULATION OF PULSE DATA BEGINS HERE.
00453 ♦
00454 2322 7F 20FC PULSE CLR ACTUAL CLEAR LOCATIONS USED DURING
00455 2325 7F 20FD CLR ACTUAL+1 ROUND-OFF ERROR CORRECTION.
00456 ♦
00457 2328 CE 20ED LDX #POWER CALCULATE CURRENT POWER FACTO
00458 232B B6 2141 LDA A PRBIAS
00459 232E F6 2142 LDA B PRBIAS+1 GET POWER CONVERSION FACTOR.
00460 ♦
00461 2331 BD 2457 JSR DIV16 CALCULATE POWER PER PULSE
00462 ♦ INTERVAL.
00463 2334 B7 20DE STA A PRFACT
00464 2337 F7 20DF STA B PRFACT+1 SAVE INTERMEDIATE RESULT.
00465 ♦
00466 233A FE 20FA LDX PULSNM
00467 233D 09 DEX MULTIPLY THE BIASED POWER
00468 233E FB 20DF LOOP1 ADD B PRFACT+1 FACTOR BY THE DESIRED
00469 2341 B9 20DE ADC A PRFACT NUMBER OF PULSES PER HALF-
00470 2344 09 DEX CYCLE.
00471 2345 26 F7 BNE LOOP1
00472 ♦
00473 2347 B7 20DE STA A PRFACT STORE CONVERTED POWER FACTOR.
00474 234A F7 20DF STA B PRFACT+1
00475 ♦
00476 234D FE 20E0 LDX SINADR INITIALIZE SINE DATA POINTER.
00477 2350 FF 20FE STX PULSX

00479	◆			
00480	◆	COMPUTE DATA FOR THE ON AND OFF TABLES.		
00481	◆			
00482 2353 BD 2443		JSR TABLE	INITIALIZE ON AND OFF TABLE	
00483 2356 20 06		BRA BEGIN	POINTERS.	
00484	◆			
00485 2358 7C 20FF	LOOP2	INC PULSX+1	NEXT SINE TABLE ADDRESS.	
00486 235B 7C 20FF		INC PULSX+1	WATCH FOR BYTE BOUNDARY!	
00487	◆			
00488 235E BD 2407	BEGIN	JSR STORE	CALCULATE AND STORE ON AND	
00489	◆		OFF INTERVALS.	
00490 2361 7A 20DD		DEC N	COUNT THE TABLE ENTRY.	
00491 2364 26 F2		BNE LOOP2	FINISH THE QUARTER CYCLE.	
00492	◆			
00493 2366 86 FF		LDA A #\$FF	PUT MAXPOS INTO A & B TO	
00494 2368 C6 FF		LDA B #\$FF	COMPUTE THE CENTER ON INTERVAL	
00495	◆			
00496 236A BD 240E		JSR STORE1	COMPUTE CENTER ON INTERVAL.	
00497	◆			
00498	◆	CORRECT FOR ROUND-OFF ERROR. FIND THE DIFFERENCE		
00499	◆	BETWEEN THE DESIRED NUMBER OF BITS PER HALF-CYCLE		
00500	◆	AND THE SUM OF THE UNCORRECTED ON AND OFF TABLE		
00501	◆	VALUES.		
00502	◆			
00503 236D B6 20FC		LDA A ACTUAL	OBTAIN THE UNCORRECTED DATA.	
00504 2370 F6 20FD		LDA B ACTUAL+1		
00505	◆			
00506 2373 E0 00		SUB B 0,X	CORRECT THE ACTUAL ON AND	
00507 2375 82 00		SBC A #\$0	OFF BIT COUNT FOR THE EXTRA	
00508 2377 E0 00		SUB B 0,X	ON AND OFF INTERVALS ADDED	
00509 2379 82 00		SBC A #\$0	BY THE LAST CALL TO THE	
00510	◆		STORE ROUTINE. XR CONT'S OFF	
00511 237B FE 2002		LDX ON		
00512 237E E0 00		SUB B 0,X	CORRECT FOR EXTRA ON INTERVAL	
00513 2380 82 00		SBC A #\$0		

00515 ◆
 00516 ◆ CALCULATE THE DIFFERENCE BETWEEN THE DESIRED
 00517 ◆ NUMBER OF BITS PER HALF-CYCLE AND THE ACTUAL
 00518 ◆ COUNT.
 00519 ◆
 00520 2382 F0 2103 SUB B HAFTOT+1 THE RESULT WILL BE A NEGATIVE
 00521 2385 B2 2102 SBC A HAFTOT NUMBER OF SMALL MAGNITUDE.
 00522 ◆
 00523 ◆ MAKE THE ACTUAL BIT COUNT EQUAL THE DESIRED
 00524 ◆ BIT COUNT BY ADDING BITS TO THE ON INTERVAL
 00525 ◆ OF PULSES, STARTING WITH THE OUTSIDE PULSE
 00526 ◆ INTERVALS.
 00527 2388 05 01 BIT B #\\$1 IS CORRECTION FACTOR EVEN
 00528 ◆ OR ODD?
 00529 238A 27 03 BEQ MORE IF EVEN, SKIP CENTER PULSE.
 00530 ◆
 00531 238C 60 00 INC 0,X ADD 1 TO THE CENTER PULSE.
 00532 238E 50 INC B CORRECT ERROR DIFFERENCE.
 00533 ◆
 00534 239F 37 MORE PSH B
 00535 2390 BD 2443 JSR TABLE START AT OUTER PULSES.
 00536 2393 33 PUL B
 00537 ◆
 00538 2394 5D LOOP3 TST B IS CORRECTION FACTOR ZERO?
 00539 2395 27 12 BEQ LOAD IF SO, LOAD DRIVER RAM.
 00540 ◆
 00541 2397 FE 20D2 LDX ON
 00542 239A 60 01 INC 1,X ADD 1 TO AN ON INTERVAL.
 00543 ◆
 00544 239C 50 INC B SUBTRACT ONE FOR EACH SIDE
 00545 239D 50 INC B FROM THE ERROR DIFFERENCE.
 00546 ◆
 00547 239E 70 20D3 INC ON+1 GO TO NEXT PULSE INTERVAL.
 00548 ◆
 00549 23A1 7A 20DD DEC N DECREMENT PULSE COUNT.
 00550 ◆
 00551 23A4 26 EE BNE LOOP3 STEP THRU PULSES IN A HALF-
 00552 ◆ CYCLE.
 00553 23A6 5D TST B TEST THE ERROR COUNT.
 00554 23A7 26 E6 BNE MORE IF THE ERROR COUNT WAS
 00555 ◆ GREATER THAN THE # OF PULSES
 00556 ◆ PER HALF-CYCLE, START ADDING
 00557 ◆ BITS AT THE OUTSIDE INTERVALS

00559	◆				
00560	◆	LOAD THE DRIVER RAM.			
00561	◆				
00562 23A9 BD 2443	LOAD	JSR	TABLE	INITIALIZE THE TABLE POINTERS	
00563	◆				
00564 23AC 7C 20D0		INC	N	INCREASE N TO INCLUDE THE	
00565	◆			CENTER PULSE.	
00566 23HF 20 06		BRA	LOOP4	ENTER LOAD LOOP.	
00567	◆				
00568 23B1 7C 20D3	TOP1	INC	DN+1	GO TO THE NEXT PULSE INTERVAL	
00569 23B4 7C 20D5		INC	OFF+1		
00570	◆				
00571 23F7 BD 26	LOOP4	BSR	Z1Z	STORE A PULSE INTERVAL'S	
00572	◆			DATA.	
00573 23B9 7A 20D0		DEC	N	COUNT THE INTERVAL.	
00574 23BC 26 F3		BNE	TOP1	LOAD UPTO THE CENTER PULSE.	
00575	◆				
00576 23BE 7A 20D3		DEC	DN+1	BACK UP ONE FROM THE CENTER	
00577 23C1 7A 20D5		DEC	OFF+1	PULSE.	
00578	◆				
00579 23C4 BD 244F		JSR	COUNT	RESET THE PULSE COUNT.	
00580 23C7 20 06		BRA	LOOPS	LOAD THE 2ND QUARTER CYCLE.	
00581	◆				
00582 23C9 7A 20D3	TOP2	DEC	DN+1	GO TO THE NEXT PULSE INTERVAL	
00583 23C0 7A 20D5		DEC	OFF+1		
00584	◆				
00585 23CF BD 0E	LOOPS	BSR	Z1Z	STORE INTERVAL PULSE DATA.	
00586 23D1 7A 20D0		DEC	N	COUNT THE PULSE INTERVAL.	
00587 23D4 26 F3		BNE	TOP2	LOAD UNTIL THE OUTSIDE PULSE.	
00588	◆				
00589	◆	SWITCH DRIVER RAM BUFFERS FOR THE PHASE			
00590	◆	CURRENTLY BEING UPDATED.			
00591	◆				
00592 23D6 B6 4002	SWITCH	LDA A	PIA1BD		
00593 23D9 98 04		EOR A	#\$4	TOGGLE BIT 2 TO SWITCH BUFFER	
00594 23DB B7 4002		STA A	PIA1BD		
00595	◆				
00596 23DE 39		RTS		FINISHED CURRENT UPDATE.	

00598	◆			
00599	◆			
00600	◆	SUBROUTINES.		
00601	◆			
00602	◆			
00603 23DF 4F	Z1Z	CLR A		PUT A ZERO IN ACCUM. A.
00604	◆			
00605 23E0 FE 20D4		LDX OFF		
00606 23E3 8D 0B		BSR LDRAM		LOAD AN OFF INTERVAL (ZERO'S)
00607	◆			
00608 23E5 86 01		LDA A #\$1		
00609 23E7 FE 20D2		LDX ON		LOAD AN ON INTERVAL (ONE'S).
00610 23EA 8D 04		BSR LDRAM		
00611	◆			
00612 23EC 4F		CLR A		
00613 23ED FE 20D4		LDX OFF		LOAD AN OFF INTERVAL (ZERO'S)
00614	◆			
00615 23F0 E6 01	LDRAM	LDA B 1,X		OBTAIN BIT COUNT TO BE LOADED
00616 23F2 FE 20E4		LDX ROTATE		GET DRIVER RAM POINTER.
00617	◆			
00618 23F5 A7 00	LOOP6	STA A 0,X		STORE A BIT.
00619 23F7 8C 0000		CPX #\$0		IS THE POINTER AT ZERO?
00620 23FA 26 03		BNE TESTB		
00621	◆			
00622 23FC FE 2100		LDX TOTAL		FOLD AROUND DRIVER RAM ADDR.
00623	◆			
00624 23FF 09	TESTB	DEX		DECREMENT POINTER.
00625 2400 5A		DEC B		COUNT THE LOADED BIT.
00626 2401 26 F2		BNE LOOP6		LOAD MORE BITS.
00627	◆			
00628 2403 FF 20E4		STX ROTATE		SAVE DRIVER RAM POINTER
00629 2406 39		RTS		FOR NEXT PULSE INTERVAL.

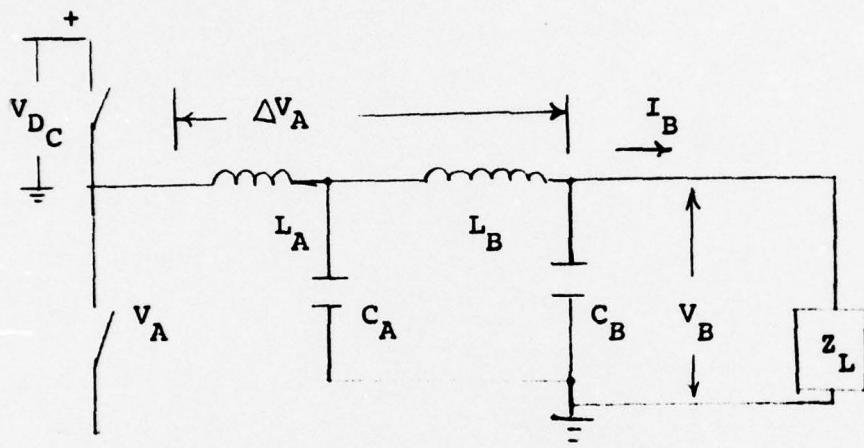
00631
 00632 ◆ THIS SUBROUTINE CALCULATES AND STORES THE ON AND
 00633 ◆ OFF INTERVALS FOR EACH PULSE INTERVAL PREPARING
 00634 ◆ FOR LOADING THE PULSE BIT PATTERN.
 00635
 00636 2407 FE 20FE STORE LDX PULSX GET THE PULSE DATA ADDRESS.
 00637 ◆
 00638 2408 A6 00 LDA A 0,X
 00639 240C E6 01 LDA B 1,X GET A SINE TABLE VALUE.
 00640 ◆
 00641 240E 7C 20D3 STORE1 INC ON+1
 00642 2411 7C 20D5 INC OFF+1 INCREMENT ON AND OFF POINTERS
 00643 ◆
 00644 2414 CE 20D6 LDX #PFRFACT GET THE CURRENT POWER FACTOR.
 00645 2417 BD 2457 JSR DIV16 CALCULATE ON INTERVAL.
 00646 2418 FB 20E3 ADD B HALFIN ADD 1/2 OF BITS PER INTERVAL.
 00647 ◆
 00648 241D FE 20D2 LDX ON GET ON TABLE POINTER.
 00649 2420 E7 00 STA B 0,X STORE ON INTERVAL.
 00650 ◆
 00651 2422 58 BSR ACCUM
 -00652 2423 80 00 BSR ACCUM ADD 2X ON INTERVAL TO ERROR
 00653 ◆ SUM.
 00654 2425 57 BSR ACCUM DIVIDE ON INTVL BY 2.
 00655 2426 50 NEG B 2'S COMP. THE ON INTERVAL.
 00656 2427 FB 20E2 ADD B INTVL ADD THE NUMBER OF BITS/INTVL.
 00657 2428 57 ASR B DIVIDE BY 2 TO GET OFF INTVL.
 00658 ◆
 00659 242B FE 20D4 LDX OFF
 00660 242E E7 00 STA B 0,X STORE THE OFF INTERVAL.
 00661 ◆
 00662 2430 58 ASL B MULTIPLY OFF INTVL BY 4.
 00663 2431 58 ASL B
 00664 ◆
 00665 2432 36 ACCUM PSH A
 00666 2433 37 PSH B
 00667 2434 FB 20FD ADD B ACTUAL+1 ACCUMULATE THE ACTUAL BITS
 00668 2437 B9 20FC ADC A ACTUAL CALCULATED PER PULSE INTERVAL
 00669 2438 B7 20FC STA A ACTUAL
 00670 243D F7 20FD STA B ACTUAL+1
 00671 2440 33 PUL B
 00672 2441 32 PUL A
 00673 2442 39 RTS
 00674 ◆
 00675 ◆
 00676 2443 CE 20AD TABLE LDX #OFFTAB-1 INITIALIZE OFF TABLE POINTE
 00677 2446 FF 20D4 STX OFF
 00678 2449 CE 20B9 LDX #ONTAB-1 INITIALIZE ON TABLE POINTER.
 00679 244C FF 20D2 STX ON
 00680 ◆
 00681 244F F6 20FB COUNT LDA B PULSNM+1 GET THE CURRENT PULSE NUMBER.
 00682 2452 57 ASR B DIVIDE BY 2.
 00683 2453 F7 20DD STA B N STORE PULSES/HALF-CYCLE.
 00684 2456 39 RTS (NOT INCLUDING CENTER PULSE).

00686 ♦ 16 BIT UNSIGNED DIVIDE (16 BIT RESULT).
 00687 ♦ A,B DIVIDED BY (X), (X+1).
 00688 ♦ RESULT IN A,B. (X), (X+1) UNCHANGED.
 00689 ♦
 00690 2457 37 DIV16 PSH B DIVIDEND TO STACK.
 00691 2458 36 PSH A
 00692 2459 A6 00 LDA A X
 00693 245B E6 01 LDA B 1,X
 00694 245D 37 PSH B DIVISOR TO STACK.
 00695 245E 36 PSH A
 00696 245F 34 DES LEAVE ROOM FOR COUNT.
 00697 2460 30 TSX (X) POINTER TO STACKED DATA.
 00698 2461 86 01 LDA A #1
 00699 2463 6D 01 TST 1,X
 00700 2465 2B 08 BMI DIV153
 00701 2467 4C DIV151 INC A
 00702 2468 68 02 ASL 2,X
 00703 246A 69 01 ROL 1,X
 00704 246C 2B 04 BMI DIV153
 00705 246E 81 11 CMP A #17
 00706 2470 26 F5 BNE DIV151
 00707 2472 A7 00 DIV153 STA A 0,X
 00708 2474 A6 03 LDA A 3,X
 00709 2476 E6 04 LDA B 4,X
 00710 2478 6F 03 CLR 3,X
 00711 247A 6F 04 CLR 4,X
 00712 ♦
 00713 247C E0 02 DIV163 SUB B 2,X
 00714 247E A2 01 SBC A 1,X
 00715 2480 24 07 BCC DIV165 DIVISOR STILL SMALL.
 00716 2482 EB 02 ADD B 2,X DIVISOR TOO LARGE.
 00717 2484 A9 01 ADC A 1,X RESTORE.
 00718 2486 0C CLC
 00719 2487 20 01 BRA DIV167
 00720 2489 0D DIV165 SEC
 00721 248A 69 04 DIV167 ROL 4,X
 00722 248C 69 03 ROL 3,X
 00723 248E 64 01 LSR 1,X ADJUST DIVISOR.
 00724 2490 66 02 RDR 2,X
 00725 2492 6A 00 DEC 0,X
 00726 2494 26 E6 BNE DIV163
 00727 ♦
 00728 2496 31 INS
 00729 2497 31 INS
 00730 2498 31 INS
 00731 2499 32 PUL A
 00732 249A 33 PUL B
 00733 249B 39 RTS
 00734 END

TOTAL ERRORS 00000

3.2.8 MATHEMATICAL ANALYSIS

3.2.8.1 REQUIREMENTS



Referencing the above circuit requirements are:

1. V_{DC} cannot exceed 200V_{DC}
2. The real voltage drop V_A peak across the inductors cannot exceed 22 volts with all other voltage drop equal to 2 volts.
3. The output power is 5000 watts into a resistive load and 6250 VA a complex load.
4. Operating frequency of 50, 60 and 400 Hz.
5. Output voltage nominally of 120 volts RMS.
6. The minimum value of the inductor shall be large enough to limit the di/dt to 10 A/microsecond during a short circuit condition.

3.2.8.2 CALCULATIONS

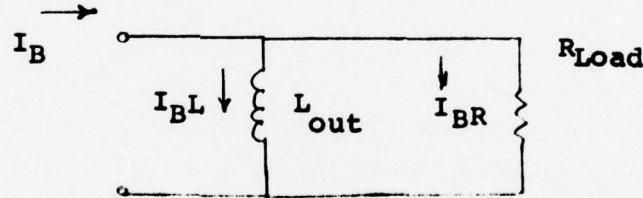
From the above requirements, the output current into a pure resistive load ($Z_L = R_L$)

$$I_B = \frac{P_B}{V_B} = 41.67 \text{ A RMS} \quad (4)$$

and the magnitude of the current for a complex load which causes a 0.8 lagging power factor is

$$I_B = \frac{P_B \text{ (complex)}}{V_B} = 52.08 \text{ A RMS} \quad (5)$$

if the load is



then $I_{BR} = I_B \text{ (Real)} = 41.67 \text{ A RMS}$

$$I_{BL} = \sqrt{I_B^2 - I_{BR}^2} \quad (6)$$

$$I_{BL} = 31.25 \text{ A RMS}$$

$$R_{\text{Load}} = \frac{V_O^2}{P_O} = 2.88 \text{ ohms} \quad (7)$$

To find the inductance needed to cause a 0.8 lagging power factor first determine X_L

$$X_L = w L_A = \frac{V_B}{I_{BL}} = 3.84 \quad (8)$$

Thus at 60Hz $L_{out} = 10.185$ millihenrys

at 50Hz $L_{out} = 12.223$ millihenrys

at 400Hz $L_{out} = 1.527$ millihenrys

As mentioned above in the requirements section the real voltage drop across inductor L_A and L_B must be less than 22 volts when the output voltage is 105% of rated voltage. At the same time the inductor must be large enough to limit the di/dt rise to 10 A/microseconds.

If it is assumed that all of the drop associated with the resistive load current is real then the maximum value of the total inductance can be found

$$X_{L_S} = X_{L_A} + X_{L_B} = \frac{\Delta V_A}{I_A \sqrt{2}} = .3734 \quad (9)$$

Thus: $L_{max} = \frac{X_{L_S}}{w}$ where $w = 2\pi f$

at 50Hz $L_{max} = 1.188$ millihenrys

at 60Hz $L_{max} = 990$ microhenrys

at 400 Hz $L_{max} = 148$ microhenrys

If indeed X_L _S is complex, its real part may be substantially less than 0.3734 ohms and the series inductance can be somewhat higher than the calculated 148 microhenrys.

The minimum value of the inductance is found using ampere's law.

$$\Delta e = L \frac{\Delta i}{\Delta t} \quad (10)$$

to drive

$$L_{min} = V_{DC} \frac{\Delta t}{\Delta i} \text{ if } \frac{\Delta i}{\Delta t} = 10 \text{ A/microsecond} \quad (11)$$

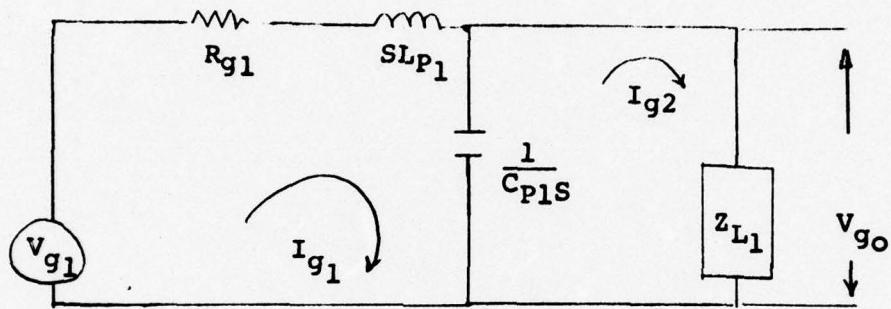
$$\text{then: } \frac{\Delta t}{\Delta i} = \frac{1}{10} \times 10^{-6}$$

$$\text{and } L_{min} = 200 \left(\frac{1}{10} \times 10^{-6} \right) \\ = 20 \text{ microhenrys}$$

For total size, weight and further reduction of $\frac{\Delta i}{\Delta t}$ a value of 50 microhenrys will be considered as the minimum series inductance value.

Now lets look at the input, output and transfer impedance.

First, the impedancies are calculated for a single section low pass filter. The simplified equivalent circuit is shown below:



$$V_{g1} = I_{g1} \left(R_{g1} + S L_{p1} + \frac{1}{C_{p1}s} \right) - \frac{1}{C_{p1}s} I_{g2} \quad (12)$$

$$0 = -\frac{1}{C_{p1}s} I_{g1} + \left(\frac{1}{C_{p1}s} + z_{L1} \right) I_{g2} \quad (13)$$

$$I_{g2} = \frac{I_{g1}}{1 + z_{L1} C_{p1}s}$$

$$z_{11} = \frac{V_{g1}}{I_{g1}} = L_{p1} C_{p1} z_{L1} \left[\frac{s^2 + \left(\frac{L_{p1} + R_{g1} z_{L1} C_{p1}}{L_{p1} C_{p1} z_{L1}} \right)}{1 + z_{L1} C_{p1}s} s + \frac{z_{L1} + R_{g1}}{L_{p1} C_{p1} z_{L1}} \right] \quad (14)$$

Where z_{11} is input impedance

Next the transfer impedance is found:

First, the output voltage is

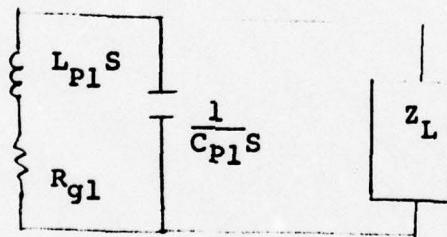
$$V_{go} = I_{g2} Z_L$$

yielding

$$\frac{V_{go}}{V_{gl}} = \frac{1}{L_{P1} C_{P1} \left[s^2 + \left(\frac{L_{P1} + R_{gl} z_{L1} C_{P1}}{L_{P1} C_{P1} z_{L1}} \right) + \frac{z_{L1} + R_{gl}}{L_{P1} C_{P1} z_{L1}} \right]} \quad (15)$$

The output impedance Z_{22} is now the parallel

Combination of

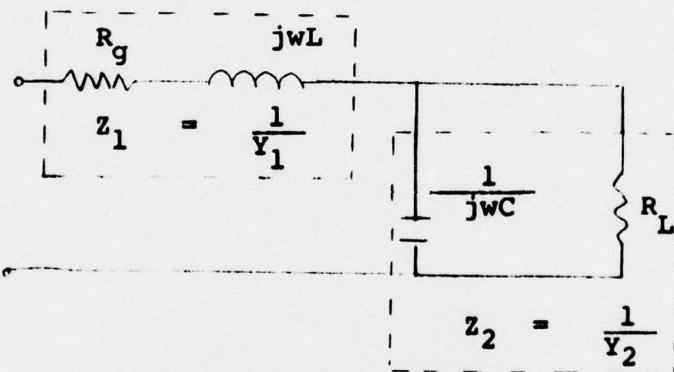


Solving yields

$$Z_{out} = \frac{\left(s + \frac{R_{gl}}{L_{P1}} \right)}{C_{P1} \left[s^2 + \frac{L_{P1} + z_{L1} C_{P1} R_{gl}}{z_{L1} C_{P1} L_{P1}} + \frac{z_{L1} + R_{gl}}{z_{L1} + C_{P1} L_{P1}} \right]} \quad (16)$$

Next we need to determine the value of the capacitor C_{PL} . The value of the capacitor is easily determined at the corner frequency. Here it is assumed that the corner frequency is 1200 hertz (the third harmonic of the 400 Hz operating frequency).

At the corner frequency the magnitudes of the impedance of the series elements and the parallel elements (shown below) must be the same. That is $z_1 = z_2$.



Thus the magnitude of the admittance must be the same.

Hence:

$$Y_1 = \frac{1}{R_g + jwL} = \frac{R_g - jwL}{R_g^2 + w^2 L^2} \quad (17)$$

$$|Y_1| = \left[\left(\frac{R_g}{R_g^2 + w^2 L^2} \right)^2 - \left(\frac{wL}{R_g^2 + w^2 L^2} \right)^2 \right]^{1/2} \quad (18)$$

and

$$Y_2 = \frac{1}{R_L} + j\omega C \quad (19)$$

$$|Y_2| = \left[\left(\frac{1}{R_L} \right)^2 - \omega^2 C^2 \right]^{1/2} \quad (20)$$

Setting $|Y_1| = |Y_2|$ we get

$$\left(\frac{R_g}{R_g^2 + \omega^2 L^2} \right)^2 - \left(\frac{\omega L}{R_g^2 + \omega^2 L^2} \right)^2 = \left(\frac{1}{R_L} \right)^2 - \omega^2 C^2$$

or

$$\omega^2 C^2 = \left(\frac{1}{R_L} \right)^2 - \frac{R_g^2 - \omega^2 L^2}{(R_g^2 + \omega^2 L^2)^2}$$

$$C = \frac{1}{\omega} \left[\left(\frac{1}{R_L} \right)^2 - \frac{R_g^2 - \omega^2 L^2}{(R_g^2 + \omega^2 C^2)^2} \right]^{1/2} \quad (21)$$

As a check on the equation if R_L is very large then $\left(\frac{1}{R_L} \right)^2$ is very small and if R_g is very small R_g^2 will be even smaller and we are left with

$$C = \frac{1}{\omega^2 L} \quad (22)$$

Note here that we only considered a resistive load. The equation becomes somewhat more complicated when a complex load is considered. The effects of other loads are being analyzed and will be presented as a supplement to this status report.

When the output is pure resistive the capacitance needed to provide a 1200 Hz corner frequency is 321 microfarads.

This value was determined using an R_g source resistance value of 0.1 ohms, an inductor value of 50 microhenrys and a load resistance of 2.88 ohms. When a 100 microhenry inductor is used the required capacitor value is 179 microfarads, and for 150 microhenrys the capacitance is 116 microfarads.

Under no load and a 50 microhenry inductor the capacitance value is 351 microfarads.

Pulse data needed for the fourier expression:

1. Pulse width
2. Center of the pulse (relative time within a cycle).

Generalized expressions:

1. Pulse width $f = \text{frequency (hz.)} . \frac{1}{4} = T = \text{Period.}$

$$\text{Width of } M^{\text{th}} \text{ pulse} = \left(\int_{\theta = 360^\circ - (\frac{N-M+1}{N}) 360^\circ}^{\theta = 360^\circ - (\frac{N-M}{N}) 360^\circ} \sin \theta d\theta \right) \frac{T}{2} \quad (23)$$

N = Number of pulses per half-cycle

M = Current pulse (Program Variable)

2. Pulse center

$$\text{Pulse center location} = T - \left(\frac{N-M}{N} \right) T - \frac{1}{2N} (T) = C$$

3. For pulse width modulation and biasing.

$$\text{Width of } M^{\text{th}} \text{ pulse} = \frac{P}{w} \quad \left\{ \begin{array}{l} \theta = 360^\circ - \left(\frac{N-M}{N} \right) 360^\circ \\ \theta = 360^\circ - \left(\frac{N-M+1}{N} \right) 360^\circ \end{array} \right. \quad \left(\frac{\sin \theta d\theta}{2} \right) \frac{T}{2} + b \quad (23)$$

P = Power factor

w = Bias divisor

b = Bias factor

$$F(jw) = \sum_{M=1}^M v_o (-1)^{\left(\frac{M-1}{N}\right)} \gamma \frac{\sin 1/2 w \gamma}{1/2 w \gamma} e^{-jw(c)} \quad (24)$$

Where $\gamma = \frac{P}{w}$

$$\begin{cases} \theta = 360^\circ - \left(\frac{N-M}{N}\right) 360^\circ \\ \theta = 360^\circ - \left(\frac{N-M+1}{N}\right) 360^\circ \end{cases}$$
$$\left(\sin \theta d\theta \right) \frac{T}{4} + b$$

And $C = T - \left(\frac{N-M}{N}\right) T = \frac{1}{2N} (T)$

An interpretation of this data is given in Figure 3.2.8-1

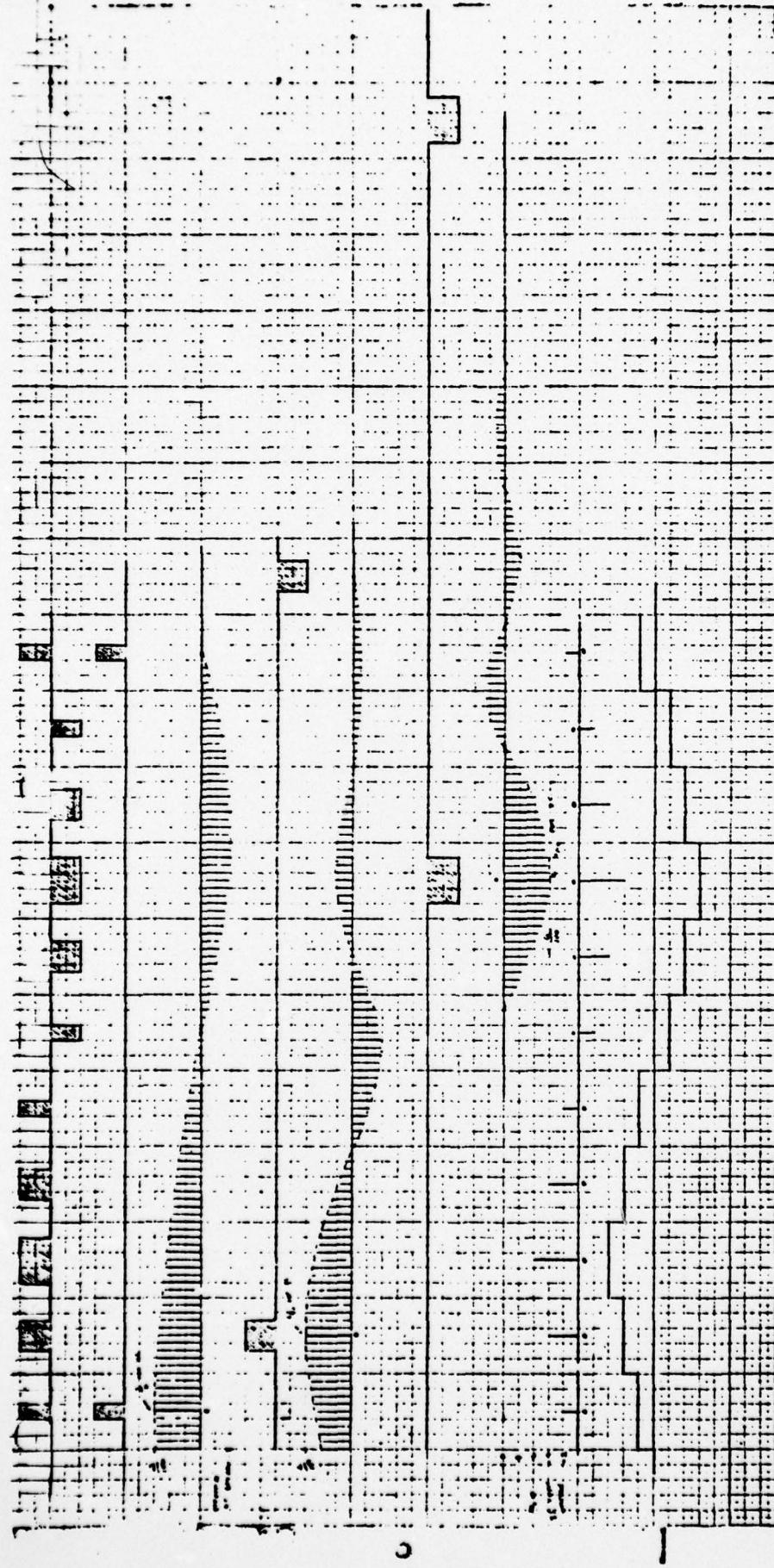


FIGURE 3.2.8-1 INTERPRETATION OF FORTIER EQUATION

3.2.8.3 COMPUTER ANALYSIS

A computer analysis of the final filter design is presented in the following section. This analysis was performed on a UNIVAC computer.

$$\text{GAIN} = 1.360500 + j0$$

NUMERATOR COEFFICIENTS - IN ASCENDING POWERS OF S

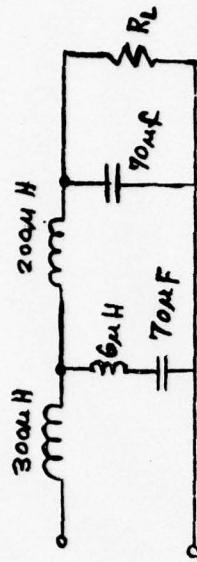
$$2.351000 + j0 \quad 0.300000 \quad 1.000000 + j0$$

DENOMINATOR ROOTS ARE

REAL PART IMAG. PART
 $-5.141373 + j0.1$ $-1.479245 + j0.4$
 $-5.141373 + j0.1$ $1.476153 + j0.4$

DENOMINATOR COEFFICIENTS - IN ASCENDING POWERS OF S

$$2.255500 + j0 \quad 3.262100 + j0 \quad 1.827700 + j0 \quad 2.005700 + j0 \quad 1.000000 + j0$$



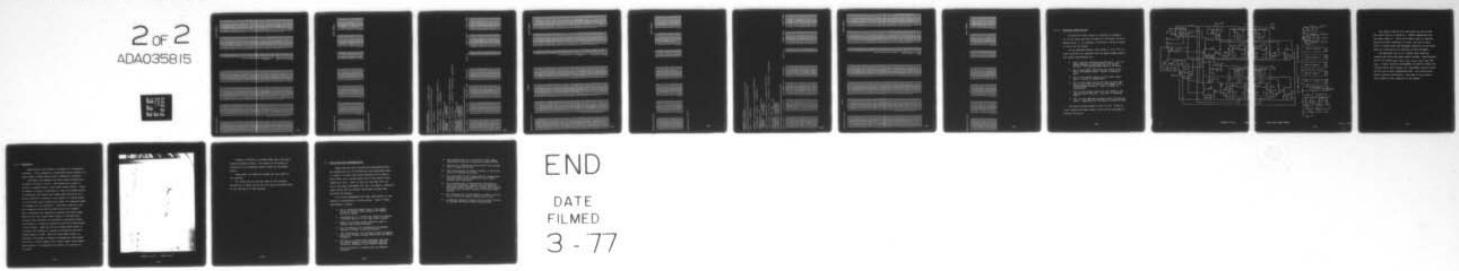
REAL PART

REAL PART	IMAGINARY PART	MAGNITUDE	PHASE (RAD)	PHASE (DEG)
1.000000 + j0.0	-1.007972 - j0.3	1.000514 + j0.0	-1.007455 - j0.3	-5.772292 - j0.2
1.000056 + j0.0	-1.075406 - j0.3	1.000591 + j0.0	-1.074771 - j0.3	-6.157989 - j0.2
1.000067 + j0.0	-1.147375 - j0.3	1.000679 + j0.0	-1.146597 - j0.3	-6.560861 + j0.2
1.000077 + j0.0	-1.224187 - j0.3	1.000779 + j0.0	-1.223234 - j0.3	-6.904771 + j0.2
1.000092 + j0.0	-1.306174 - j0.3	1.000924 + j0.0	-1.305027 - j0.3	-7.287710 + j0.2
1.000093 + j0.0	-1.395693 - j0.3	1.000932 + j0.0	-1.394857 - j0.3	-7.668794 + j0.2
1.000095 + j0.0	-1.487126 - j0.3	1.000957 + j0.0	-1.485484 - j0.3	-8.052554 + j0.2
1.000102 + j0.0	-1.586821 - j0.3	1.000964 + j0.0	-1.584215 - j0.3	-8.422459 + j0.2
1.000103 + j0.0	-1.693742 - j0.3	1.001034 + j0.0	-1.692159 - j0.3	-8.785706 + j0.2
1.000107 + j0.0	-1.801747 + j0.3	1.001174 + j0.0	-1.800482 - j0.3	-9.149120 + j0.2
1.000117 + j0.0	-1.902917 + j0.3	1.001257 + j0.0	-1.902487 - j0.3	-9.511111 + j0.2
1.000125 + j0.0	-1.995195 + j0.3	1.001345 + j0.0	-1.994684 - j0.3	-9.874102 + j0.2
1.000134 + j0.0	-2.080174 + j0.3	1.001434 + j0.0	-2.079584 - j0.3	-10.232412 + j0.2
1.000142 + j0.0	-2.165917 + j0.3	1.001522 + j0.0	-2.165295 - j0.3	-10.586706 + j0.2
1.000151 + j0.0	-2.249746 + j0.3	1.001611 + j0.0	-2.249045 - j0.3	-10.940195 + j0.2
1.000160 + j0.0	-2.333575 + j0.3	1.001700 + j0.0	-2.332854 - j0.3	-11.293584 + j0.2
1.000169 + j0.0	-2.416404 + j0.3	1.001789 + j0.0	-2.415683 - j0.3	-11.647192 + j0.2
1.000178 + j0.0	-2.499233 + j0.3	1.001878 + j0.0	-2.498512 - j0.3	-12.000771 + j0.2
1.000187 + j0.0	-2.581962 + j0.3	1.001967 + j0.0	-2.578241 - j0.3	-12.353967 + j0.2
1.000196 + j0.0	-2.664691 + j0.3	1.002056 + j0.0	-2.662970 - j0.3	-12.707135 + j0.2
1.000205 + j0.0	-2.747420 + j0.3	1.002145 + j0.0	-2.745682 - j0.3	-13.060323 + j0.2
1.000214 + j0.0	-2.830149 + j0.3	1.002234 + j0.0	-2.827451 - j0.3	-13.413511 + j0.2
1.000223 + j0.0	-2.912878 + j0.3	1.002323 + j0.0	-2.909720 - j0.3	-13.766699 + j0.2
1.000232 + j0.0	-2.995607 + j0.3	1.002412 + j0.0	-2.987989 - j0.3	-14.119887 + j0.2
1.000241 + j0.0	-3.078336 + j0.3	1.002501 + j0.0	-3.076768 - j0.3	-14.473075 + j0.2
1.000250 + j0.0	-3.161065 + j0.3	1.002590 + j0.0	-3.159447 - j0.3	-14.826263 + j0.2
1.000259 + j0.0	-3.243794 + j0.3	1.002679 + j0.0	-3.242176 - j0.3	-15.179451 + j0.2
1.000268 + j0.0	-3.326523 + j0.3	1.002768 + j0.0	-3.324905 - j0.3	-15.532639 + j0.2
1.000277 + j0.0	-3.409252 + j0.3	1.002857 + j0.0	-3.407583 - j0.3	-15.885827 + j0.2
1.000286 + j0.0	-3.491981 + j0.3	1.002946 + j0.0	-3.480961 - j0.3	-16.239015 + j0.2
1.000295 + j0.0	-3.574710 + j0.3	1.003035 + j0.0	-3.568339 - j0.3	-16.592193 + j0.2
1.000304 + j0.0	-3.657439 + j0.3	1.003124 + j0.0	-3.655717 - j0.3	-16.945381 + j0.2
1.000313 + j0.0	-3.740168 + j0.3	1.003213 + j0.0	-3.738095 - j0.3	-17.298569 + j0.2
1.000322 + j0.0	-3.822897 + j0.3	1.003302 + j0.0	-3.816473 - j0.3	-17.651757 + j0.2
1.000331 + j0.0	-3.905626 + j0.3	1.003391 + j0.0	-3.894851 - j0.3	-18.004945 + j0.2
1.000340 + j0.0	-3.988355 + j0.3	1.003480 + j0.0	-3.973229 - j0.3	-18.358133 + j0.2
1.000349 + j0.0	-4.071084 + j0.3	1.003569 + j0.0	-4.059607 - j0.3	-18.711321 + j0.2
1.000358 + j0.0	-4.153813 + j0.3	1.003658 + j0.0	-4.147985 - j0.3	-19.064509 + j0.2
1.000367 + j0.0	-4.236542 + j0.3	1.003747 + j0.0	-4.225363 - j0.3	-19.417697 + j0.2
1.000376 + j0.0	-4.319271 + j0.3	1.003836 + j0.0	-4.307742 - j0.3	-19.770885 + j0.2
1.000385 + j0.0	-4.391999 + j0.3	1.003925 + j0.0	-4.376120 - j0.3	-20.124073 + j0.2
1.000394 + j0.0	-4.474728 + j0.3	1.004014 + j0.0	-4.455498 - j0.3	-20.477261 + j0.2
1.000403 + j0.0	-4.557457 + j0.3	1.004103 + j0.0	-4.536866 - j0.3	-20.830449 + j0.2
1.000412 + j0.0	-4.640186 + j0.3	1.004192 + j0.0	-4.618234 - j0.3	-21.183637 + j0.2
1.000421 + j0.0	-4.722915 + j0.3	1.004281 + j0.0	-4.699502 - j0.3	-21.536825 + j0.2
1.000430 + j0.0	-4.805644 + j0.3	1.004370 + j0.0	-4.780770 - j0.3	-21.889013 + j0.2
1.000439 + j0.0	-4.888373 + j0.3	1.004459 + j0.0	-4.862038 - j0.3	-22.242191 + j0.2
1.000448 + j0.0	-4.971102 + j0.3	1.004548 + j0.0	-4.943306 - j0.3	-22.594379 + j0.2
1.000457 + j0.0	-5.053831 + j0.3	1.004637 + j0.0	-5.024574 - j0.3	-22.946567 + j0.2
1.000466 + j0.0	-5.136560 + j0.3	1.004726 + j0.0	-5.105842 - j0.3	-23.298755 + j0.2
1.000475 + j0.0	-5.219289 + j0.3	1.004815 + j0.0	-5.187110 - j0.3	-23.650943 + j0.2
1.000484 + j0.0	-5.301998 + j0.3	1.004904 + j0.0	-5.268378 - j0.3	-24.003131 + j0.2
1.000493 + j0.0	-5.384727 + j0.3	1.004993 + j0.0	-5.359646 - j0.3	-24.355319 + j0.2
1.000502 + j0.0	-5.467456 + j0.3	1.005082 + j0.0	-5.440914 - j0.3	-24.707507 + j0.2
1.000511 + j0.0	-5.550185 + j0.3	1.005171 + j0.0	-5.522182 - j0.3	-25.059695 + j0.2
1.000520 + j0.0	-5.632914 + j0.3	1.005260 + j0.0	-5.603450 - j0.3	-25.411883 + j0.2
1.000529 + j0.0	-5.715643 + j0.3	1.005349 + j0.0	-5.684718 - j0.3	-25.764071 + j0.2
1.000538 + j0.0	-5.798372 + j0.3	1.005438 + j0.0	-5.766086 - j0.3	-26.116259 + j0.2
1.000547 + j0.0	-5.881101 + j0.3	1.005527 + j0.0	-5.847354 - j0.3	-26.468447 + j0.2
1.000556 + j0.0	-5.963830 + j0.3	1.005616 + j0.0	-5.928622 - j0.3	-26.820635 + j0.2
1.000565 + j0.0	-6.046559 + j0.3	1.005705 + j0.0	-6.010890 - j0.3	-27.172823 + j0.2
1.000574 + j0.0	-6.129288 + j0.3	1.005794 + j0.0	-6.092158 - j0.3	-27.525011 + j0.2
1.000583 + j0.0	-6.212017 + j0.3	1.005883 + j0.0	-6.173426 - j0.3	-27.877199 + j0.2
1.000592 + j0.0	-6.294746 + j0.3	1.005972 + j0.0	-6.254694 - j0.3	-28.229387 + j0.2
1.000601 + j0.0	-6.377475 + j0.3	1.006061 + j0.0	-6.335962 - j0.3	-28.581575 + j0.2
1.000610 + j0.0	-6.460204 + j0.3	1.006150 + j0.0	-6.417230 - j0.3	-28.933763 + j0.2
1.000619 + j0.0	-6.542933 + j0.3	1.006239 + j0.0	-6.498508 - j0.3	-29.285951 + j0.2
1.000628 + j0.0	-6.625662 + j0.3	1.006328 + j0.0	-6.579776 - j0.3	-29.638139 + j0.2
1.000637 + j0.0	-6.708391 + j0.3	1.006417 + j0.0	-6.661044 - j0.3	-30.000327 + j0.2
1.000646 + j0.0	-6.791120 + j0.3	1.006506 + j0.0	-6.742312 - j0.3	-30.352515 + j0.2
1.000655 + j0.0	-6.873849 + j0.3	1.006595 + j0.0	-6.823580 - j0.3	-30.704703 + j0.2
1.000664 + j0.0	-6.956578 + j0.3	1.006684 + j0.0	-6.904848 - j0.3	-31.056891 + j0.2
1.000673 + j0.0	-7.039307 + j0.3	1.006773 + j0.0	-7.086116 - j0.3	-31.409079 + j0.2
1.000682 + j0.0	-7.122036 + j0.3	1.006862 + j0.0	-7.167384 - j0.3	-31.761267 + j0.2
1.000691 + j0.0	-7.204765 + j0.3	1.006951 + j0.0	-7.248652 - j0.3	-32.113455 + j0.2
1.000700 + j0.0	-7.287494 + j0.3	1.007040 + j0.0	-7.329920 - j0.3	-32.465643 + j0.2
1.000709 + j0.0	-7.370223 + j0.3	1.007129 + j0.0	-7.411188 - j0.3	-32.817831 + j0.2
1.000718 + j0.0	-7.452952 + j0.3	1.007218 + j0.0	-7.492466 - j0.3	-33.160019 + j0.2
1.000727 + j0.0	-7.535681 + j0.3	1.007307 + j0.0	-7.573744 - j0.3	-33.512207 + j0.2
1.000736 + j0.0	-7.618410 + j0.3	1.007396 + j0.0	-7.655022 - j0.3	-33.864395 + j0.2
1.000745 + j0.0	-7.691139 + j0.3	1.007485 + j0.0	-7.736300 - j0.3	-34.216583 + j0.2
1.000754 + j0.0	-7.773868 + j0.3	1.007574 + j0.0	-7.817578 - j0.3	-34.568771 + j0.2
1.000763 + j0.0	-7.856597 + j0.3	1.007663 + j0.0	-7.898856 - j0.3	-34.920959 + j0.2
1.000772 + j0.0	-7.939326 + j0.3	1.007752 + j0.0	-7.980134 - j0.3	-35.273147 + j0.2
1.000781 + j0.0	-8.022055 + j0.3	1.007841 + j0.0	-8.071412 - j0.3	-35.625335 + j0.2
1.000790 + j0.0	-8.104784 + j0.3	1.007930 + j0.0	-8.162690 - j0.3	-35.977523 + j0.2
1.000799 + j0.0	-8.187513 + j0.3	1.008019 + j0.0	-8.253968 - j0.3	-36.329711 + j0.2
1.000808 + j0.0	-8.270242 + j0.3	1.008108 + j0.0	-8.345236 - j0.3	-36.681899 + j0.2
1.000817 + j0.0	-8.352971 + j0.3	1.008197 + j0.0	-8.436504 - j0.3	-37.034087 + j0.2
1.000826 + j0.0	-8.435700 + j0.3	1.008286 + j0.0	-8.527772 - j0.3	-37.386275 + j0.2
1.000835 + j0.0	-8.518429 + j0.3	1.008375 + j0.0	-8.618840 - j0.3	-37.738463 + j0.2
1.000844 + j0.0	-8.591158 + j0.3	1.008464 + j0.0	-8.710108 - j0.3	-38.090651 + j0.2
1.000853 + j0.0	-8.673887 + j0.3	1.008553 + j0.0	-8.801376 - j0.3	-38.442839 + j0.2
1.000862 + j0.0	-8.756616 + j0.3	1.008642 + j0.0	-8.892644 - j0.3	-38.795027 + j0.2
1.000871 + j0.0	-8.839345 + j0.3	1.008731 + j0.0	-8.983912 - j0.3	-39.147215 + j0.2
1.000880 + j0.0	-8.922074 + j0.3	1.008820 + j0.0	-9.075180 - j0.3	-39.499393 + j0.2
1.000889 + j0.0	-9.004803 + j0.3	1.008909 + j0.0	-9.166448 - j0.3	-39.851581 + j0.2
1.000898 + j0.0	-9.087532 + j0.3	1.009098 + j0.0	-9.257716 - j0.3	-40.203769 + j0.2
1.000907 + j0.0	-9.170261 + j0.3	1.009187 + j0.0	-9.348984 - j0.3	-40.555957 + j0.2
1.000916 + j0.0	-9.252990 + j0.3	1.009276 + j0.0	-9.440252 - j0.3	-40.908145 + j0.2
1.000925 + j0.0	-9.335719 + j0.3	1.009365 + j0.0	-9.531520 - j0.3	-41.260333 + j0.2
1.000934 + j0.0	-9.418448 + j0.3	1.009454 + j0.0	-9.622788 - j0.3	-41.612521 + j0.2
1.000943 + j0.0	-9.491177 + j0.3	1.009543 + j0.0	-9.714056 - j0.3	-41.964709 + j0.2
1.000952 + j0.0	-9.573906 + j0.3	1.009632 + j0.0	-9.805324 - j0.3	-42.316897 + j0.2
1.000961 + j0.0	-9.656635 + j0.3	1.009721 + j0.0	-9.896592 - j0.3	-42.669085 + j0.2
1.000970 + j0.0	-9.739364 + j0.3	1.009810 + j0.0	-9.987860 - j0.3	-43.021273 + j0.2
1.000979 + j0.0	-9.822093 + j0.3	1.0099 + j0.0	-1.009128 - j0.3	-43.373461 + j0.2
1.000988 + j0.0	-9.904822 + j0.3	1.009999 + j0.0	-1.000436 - j0.3	-43.725649 + j0.2
1.000997 + j0.0	-9.987551 + j0.3	1.001000 + j0.0	-1.001744 - j0.3	-44.077837 + j0.2
1.001006 + j0.0	-1.000480 + j0.3	1.001001 +		

AD-A035 815 MOTOROLA INC PHOENIX ARIZ SEMICONDUCTOR PRODUCTS DIV F/G 10/2
DEVELOPMENT OF AN INTEGRATED POWER MODULE INVERTER.(U)
OCT 76 DAAK02-75-C-0101

UNCLASSIFIED NL

2 OF 2
ADA035815



END

DATE
FILMED
3 - 77

INVERTER PROJECT

DATF 090876

661NS*EE48U.FRES

UNIVERSITY PROJECT

DATE 090876

IEEE 11854-2014(E) SP

FREQUENCY RESPONSE
PROBLEM IDENTIFICATION - JSG INVERTER PROJECT

GAIN = 1.3e500+00

NUMERATOR COEFFICIENTS - IN ASCENDING POWERS OF S

2.381000+09 0.000000 1.000000+00

NUMERATOR ROOTS ARE

REAL PART IMAG. PART
0.000000 -4.876549+04
0.000000 4.379549+C4

DEMONINATOR COEFFICIENTS - IN ASCENDING POWERS OF S

2.0240500+15 5.027e00+11 1.e27900+08 4.965200+03 1.000000+00

DEMONINATOR ROOTS ARE

REAL PART IMAG. PART
-7.92095+04 -1.e49529+04
-7.92095+04 -1.e49529+04
-1.090005+03 -4.e2003+9+03
-1.090005+03 4.e2003+9+03

RADIAN. FREQ.	REAL PART	IMAGINARY PART	MAGNITUDE	PHASE. DB	PHASE (RAD)	PHASE (DEG)
1.000000+00	9.99035-01	-1.736873-02	1.0000054+00	-1.736865-02	-9.951509-01	-9.951509-01
1.013755+02	9.99939-01	-1.e8576907-02	1.000115-00	-1.052889-02	-1.032560+00	-1.032560+00
1.021910+02	1.e990623+00	-1.e976907-02	1.000175-00	-1.0408975-02	-1.0208975-02	-1.0208975-02
1.029375+02	1.0000707+00	-1.e96140-02	1.000248-00	-1.0409779-02	-1.010409779-02	-1.010409779-02
1.039137+02	1.0001535+00	-2.e950258-02	1.000316-00	-1.0409755-02	-1.0240005-02	-1.0240005-02
1.0471930+02	1.0002093+00	-2.e940863-02	1.000343-00	-1.0409454-02	-1.057314464-02	-1.057314464-02
1.0570961+02	1.0002747+00	-2.e9316947-02	1.0003796-00	-1.0409456-02	-1.01049456-02	-1.01049456-02
1.0670785+02	1.0003491+00	-2.e9214094-02	1.0004156-00	-1.0409457-02	-1.0240007-02	-1.0240007-02
1.0760169+02	1.0004265+00	-2.e9111745-02	1.0004534-00	-1.0409458-02	-1.035917680-02	-1.035917680-02
1.0850555+02	1.0005074+00	-2.e900834-02	1.0004915-00	-1.0409459-02	-1.045761905-02	-1.045761905-02
1.0941429+02	1.0005826+00	-2.e890593-02	1.0005294-00	-1.0409460-02	-1.055761942-02	-1.055761942-02
1.1032369+02	1.0006670+00	-2.e880352-02	1.0005674-00	-1.0409461-02	-1.065761971-02	-1.065761971-02
1.1123314+02	1.0007510+00	-2.e870111-02	1.0006053-00	-1.0409462-02	-1.075761999-02	-1.075761999-02
1.1214259+02	1.0008345+00	-2.e860870-02	1.0006432-00	-1.0409463-02	-1.085762028-02	-1.085762028-02
1.1305204+02	1.0009176+00	-2.e850629-02	1.0006811-00	-1.0409464-02	-1.095762057-02	-1.095762057-02
1.1396149+02	1.0009999+00	-2.e840388-02	1.0007190-00	-1.0409465-02	-1.105762086-02	-1.105762086-02
1.1487094+02	1.0010823+00	-2.e830147-02	1.0007579-00	-1.0409466-02	-1.115762115-02	-1.115762115-02
1.1578039+02	1.0011647+00	-2.e820906-02	1.0007968-00	-1.0409467-02	-1.125762144-02	-1.125762144-02
1.1668984+02	1.0012471+00	-2.e810665-02	1.0008357-00	-1.0409468-02	-1.135762173-02	-1.135762173-02
1.1759929+02	1.0013295+00	-2.e800424-02	1.0008746-00	-1.0409469-02	-1.145762202-02	-1.145762202-02
1.1850874+02	1.0014119+00	-2.e790183-02	1.0009135-00	-1.0409470-02	-1.155762231-02	-1.155762231-02
1.1941818+02	1.0014943+00	-2.e780942-02	1.0009524-00	-1.0409471-02	-1.165762260-02	-1.165762260-02
1.2032763+02	1.0015767+00	-2.e770701-02	1.0010013-00	-1.0409472-02	-1.175762289-02	-1.175762289-02
1.2123707+02	1.0016591+00	-2.e760459-02	1.0010402-00	-1.0409473-02	-1.185762318-02	-1.185762318-02
1.2214652+02	1.0017415+00	-2.e750218-02	1.0010791-00	-1.0409474-02	-1.195762347-02	-1.195762347-02
1.2305596+02	1.0018239+00	-2.e740077-02	1.0011180-00	-1.0409475-02	-1.205762376-02	-1.205762376-02
1.2396540+02	1.0019063+00	-2.e730836-02	1.0011569-00	-1.0409476-02	-1.215762405-02	-1.215762405-02
1.2487484+02	1.0019887+00	-2.e720595-02	1.0011958-00	-1.0409477-02	-1.225762434-02	-1.225762434-02
1.2578428+02	1.0020711+00	-2.e710354-02	1.0012347-00	-1.0409478-02	-1.235762463-02	-1.235762463-02
1.2669372+02	1.0021535+00	-2.e700113-02	1.0012736-00	-1.0409479-02	-1.245762492-02	-1.245762492-02
1.2760316+02	1.0022359+00	-2.e690872-02	1.0013125-00	-1.0409480-02	-1.255762521-02	-1.255762521-02
1.2851260+02	1.0023183+00	-2.e680631-02	1.0013514-00	-1.0409481-02	-1.265762550-02	-1.265762550-02
1.2942204+02	1.0023997+00	-2.e670390-02	1.0013803-00	-1.0409482-02	-1.275762579-02	-1.275762579-02
1.3033148+02	1.0024821+00	-2.e660149-02	1.0014192-00	-1.0409483-02	-1.285762608-02	-1.285762608-02
1.3124092+02	1.0025645+00	-2.e650008-02	1.0014581-00	-1.0409484-02	-1.295762637-02	-1.295762637-02
1.3215036+02	1.0026469+00	-2.e640067-02	1.0014970-00	-1.0409485-02	-1.305762666-02	-1.305762666-02
1.3305980+02	1.0027293+00	-2.e630026-02	1.0015359-00	-1.0409486-02	-1.315762695-02	-1.315762695-02
1.3396924+02	1.0028117+00	-2.e620085-02	1.0015748-00	-1.0409487-02	-1.325762724-02	-1.325762724-02
1.3487868+02	1.0028941+00	-2.e610044-02	1.0016137-00	-1.0409488-02	-1.335762753-02	-1.335762753-02
1.3578812+02	1.0029765+00	-2.e600003-02	1.0016526-00	-1.0409489-02	-1.345762782-02	-1.345762782-02
1.3669756+02	1.0030589+00	-2.e590062-02	1.0016915-00	-1.0409490-02	-1.355762811-02	-1.355762811-02
1.3760700+02	1.0031413+00	-2.e580021-02	1.0017304-00	-1.0409491-02	-1.365762840-02	-1.365762840-02
1.3851644+02	1.0032237+00	-2.e570080-02	1.0017693-00	-1.0409492-02	-1.375762869-02	-1.375762869-02
1.3942588+02	1.0033061+00	-2.e560039-02	1.0018082-00	-1.0409493-02	-1.385762898-02	-1.385762898-02
1.4033532+02	1.0033885+00	-2.e550008-02	1.0018471-00	-1.0409494-02	-1.395762927-02	-1.395762927-02
1.4124476+02	1.0034709+00	-2.e540067-02	1.0018860-00	-1.0409495-02	-1.405762956-02	-1.405762956-02
1.4215420+02	1.0035533+00	-2.e530026-02	1.0019249-00	-1.0409496-02	-1.415762985-02	-1.415762985-02
1.4306364+02	1.0036357+00	-2.e520085-02	1.0019638-00	-1.0409497-02	-1.425763014-02	-1.425763014-02
1.4397308+02	1.0037181+00	-2.e510044-02	1.0020027-00	-1.0409498-02	-1.435763043-02	-1.435763043-02
1.4488252+02	1.0037905+00	-2.e500003-02	1.0020416-00	-1.0409499-02	-1.445763072-02	-1.445763072-02
1.4579196+02	1.0038729+00	-2.e490062-02	1.0020805-00	-1.0409500-02	-1.455763101-02	-1.455763101-02
1.4670140+02	1.0039553+00	-2.e480021-02	1.0021194-00	-1.0409501-02	-1.465763130-02	-1.465763130-02
1.4761084+02	1.0040377+00	-2.e470080-02	1.0021583-00	-1.0409502-02	-1.475763159-02	-1.475763159-02
1.4851228+02	1.0041201+00	-2.e460039-02	1.0021972-00	-1.0409503-02	-1.485763188-02	-1.485763188-02
1.4942172+02	1.0042025+00	-2.e450008-02	1.0022361-00	-1.0409504-02	-1.495763217-02	-1.495763217-02
1.5033116+02	1.0042849+00	-2.e440067-02	1.0022750-00	-1.0409505-02	-1.505763246-02	-1.505763246-02
1.5124060+02	1.0043673+00	-2.e430026-02	1.0023139-00	-1.0409506-02	-1.515763275-02	-1.515763275-02
1.5214994+02	1.0044497+00	-2.e420085-02	1.0023528-00	-1.0409507-02	-1.525763304-02	-1.525763304-02
1.5305938+02	1.0045321+00	-2.e410044-02	1.0023917-00	-1.0409508-02	-1.535763333-02	-1.535763333-02
1.5396882+02	1.0046145+00	-2.e400003-02	1.0024306-00	-1.0409509-02	-1.545763362-02	-1.545763362-02
1.5487826+02	1.0046969+00	-2.e390062-02	1.0024695-00	-1.0409510-02	-1.555763391-02	-1.555763391-02
1.5578770+02	1.0047793+00	-2.e380021-02	1.0025084-00	-1.0409511-02	-1.565763420-02	-1.565763420-02
1.5669714+02	1.0048617+00	-2.e370080-02	1.0025473-00	-1.0409512-02	-1.575763449-02	-1.575763449-02
1.5760658+02	1.0049441+00	-2.e360039-02	1.0025862-00	-1.0409513-02	-1.585763478-02	-1.585763478-02
1.5851602+02	1.0050265+00	-2.e350008-02	1.0026251-00	-1.0409514-02	-1.595763507-02	-1.595763507-02
1.5942546+02	1.0051089+00	-2.e340067-02	1.0026640-00	-1.0409515-02	-1.605763536-02	-1.605763536-02
1.6033490+02	1.0051913+00	-2.e330026-02	1.0027029-00	-1.0409516-02	-1.615763565-02	-1.615763565-02
1.6124434+02	1.0052737+00	-2.e320085-02	1.0027418-00	-1.0409517-02	-1.625763594-02	-1.625763594-02
1.6215378+02	1.0053561+00	-2.e310044-02	1.0027807-00	-1.0409518-02	-1.635763623-02	-1.635763623-02
1.6306322+02	1.0054385+00	-2.e300003-02	1.0028196-00	-1.0409519-02	-1.645763652-02	-1.645763652-02
1.6397266+02	1.0055209+00	-2.e290062-02	1.0028585-00	-1.0409520-02	-1.655763681-02	-1.655763681-02
1.6488210+02	1.0056033+00	-2.e280021-02	1.0028974-00	-1.0409521-02	-1.665763710-02	-1.665763710-02
1.6579154+02	1.0056857+00	-2.e270080-02	1.0029363-00	-1.0409522-02	-1.675763739-02	-1.675763739-02
1.6670098+02	1.0057681+00	-2.e260039-02	1.0029752-00	-1.0409523-02	-1.685763768-02	-1.685763768-02
1.6761042+02	1.0058505+00	-2.e250008-02	1.0030141-00	-1.0409524-02	-1.695763797-02	-1.695763797-02
1.6851986+02	1.0059329+00	-2.e240067-02	1.0030530-00	-1.0409525-02	-1.705763826-02	-1.705763826-02
1.6942930+02	1.0060153+00	-2.e230026-02	1.0030919-00	-1.0409526-02	-1.715763855-02	-1.715763855-02
1.7033874+02	1.0060977+00	-2.e220085-02	1.0031308-00	-1.0409527-02	-1.725763884-02	-1.725763884-02
1.7124818+02	1.0061801+00	-2.e210044-02	1.0031697-00	-1.0409528-02	-1.735763913-02	-1.735763913-02
1.7215762+02	1.0062625+00	-2.e200003-02	1.0032086-00	-1.0409529-02	-1.745763942-02	-1.745763942-02
1.7306706+02	1.0063449+00	-2.e190062-02	1.0032475-00	-1.0409530-02	-1.755763971-02	-1.755763971-02
1.7397650+02	1.0064279+00	-2.e180021-02	1.0032			

INVENTER PROJECT

DATE 090876

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3.2.9.0 AUXILIARY POWER SECTION

An auxiliary power supply is required to generate all of the logic and bias voltages for the power circuits. Additionally, it is necessary to provide a 400 Hz AC wave to drive the fan motors.

In the proposed design (See Figure 3.2.9-1) all of these functions are supplied from one power supply module. The output requirements are:

1. Three supplies isolated with ± 6 volts. One of these supplies is required for each switch section. The maximum power here is 36 watts.
2. One +6 volt power source for the logic in the three IPS modules about 3 watts is required here.
3. One +5 volt power source for all other logic. About 15 watts is needed here.
4. One -5 volt power source for bias in the feedback circuit and for bias on the PROMS in the microprocessor section. Only 0.5 watts is needed here.
5. One +12 volt power source for the PROMS in the microprocessor section. One watt is required here.
6. Two 120 volt RMS 400 Hz power source for the fan motor. Approximately 200 watts is required here.

The total wattage needed is 255.5 watts. Based on these figures the power supply front end was designed to deliver 300 watts.

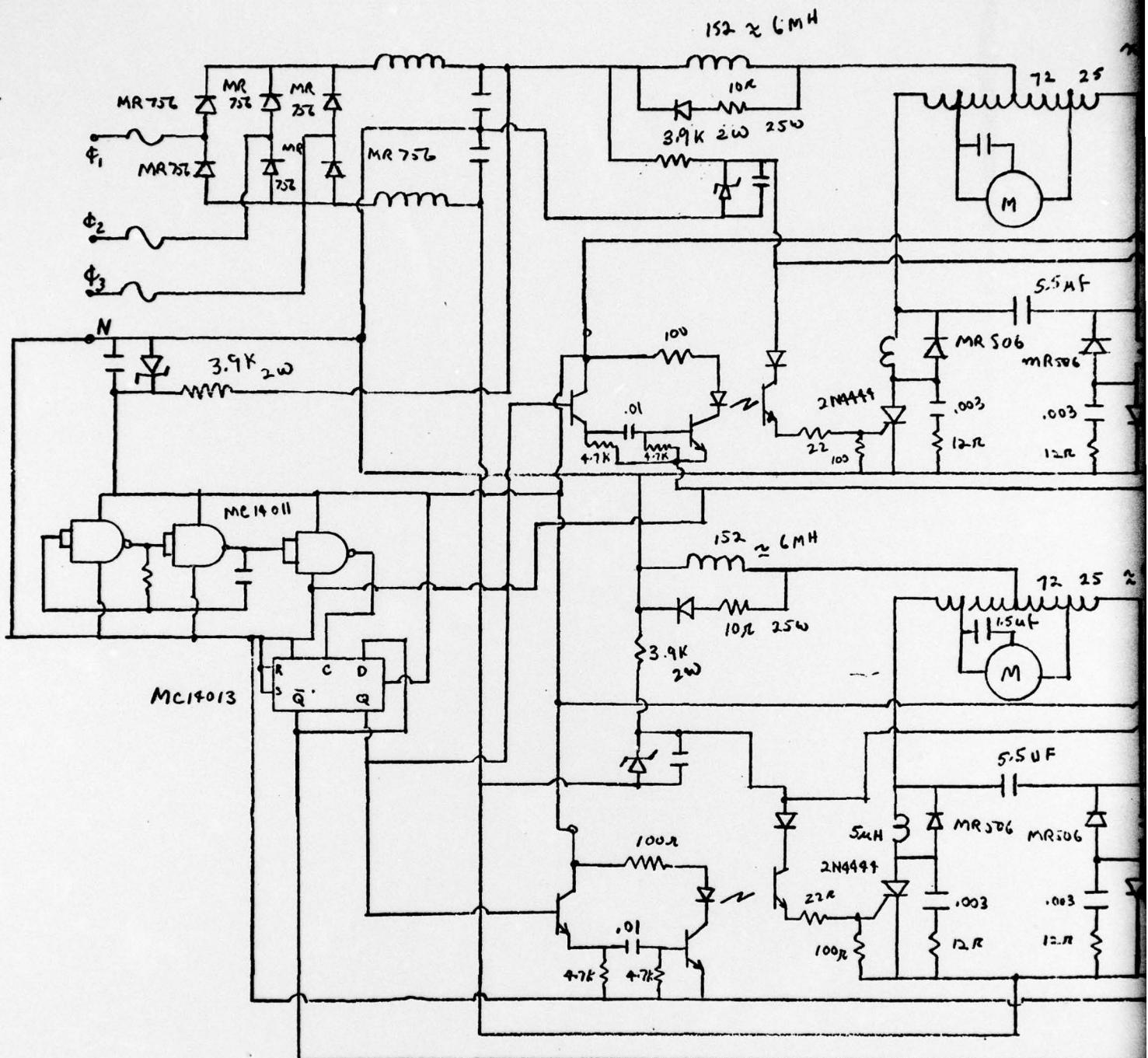
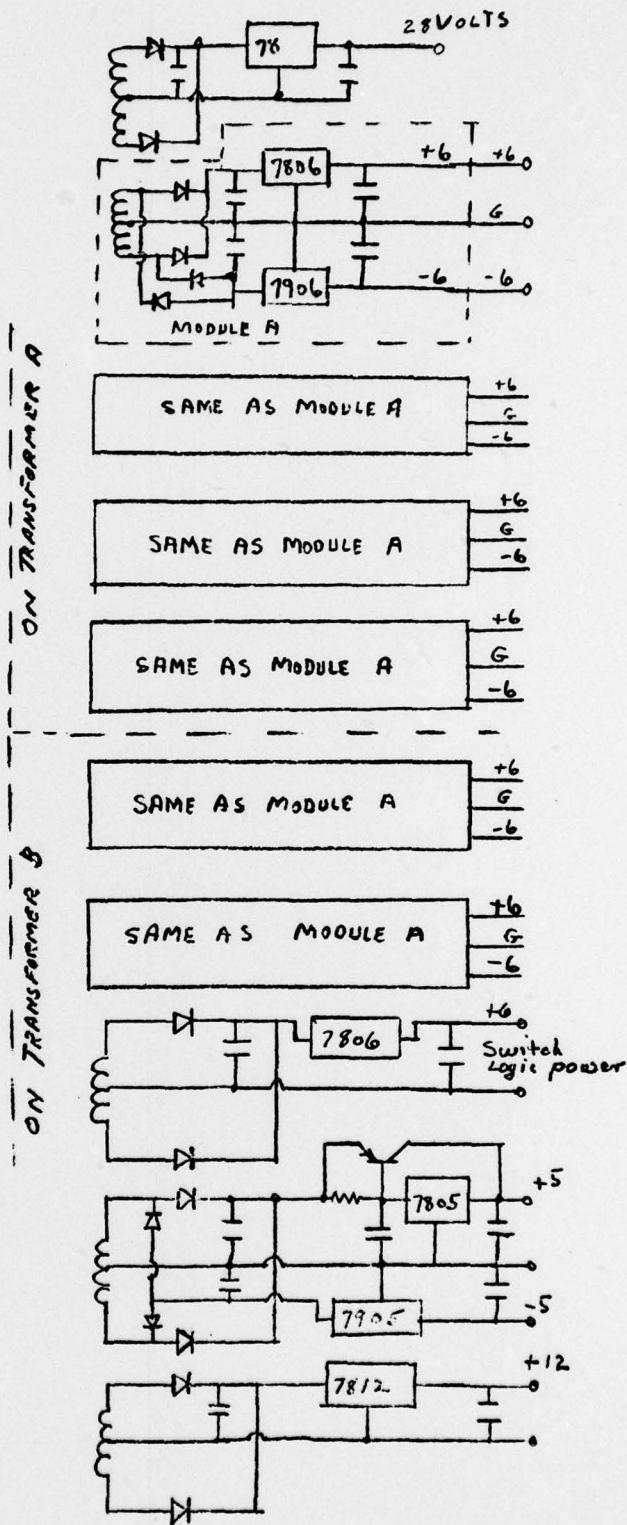
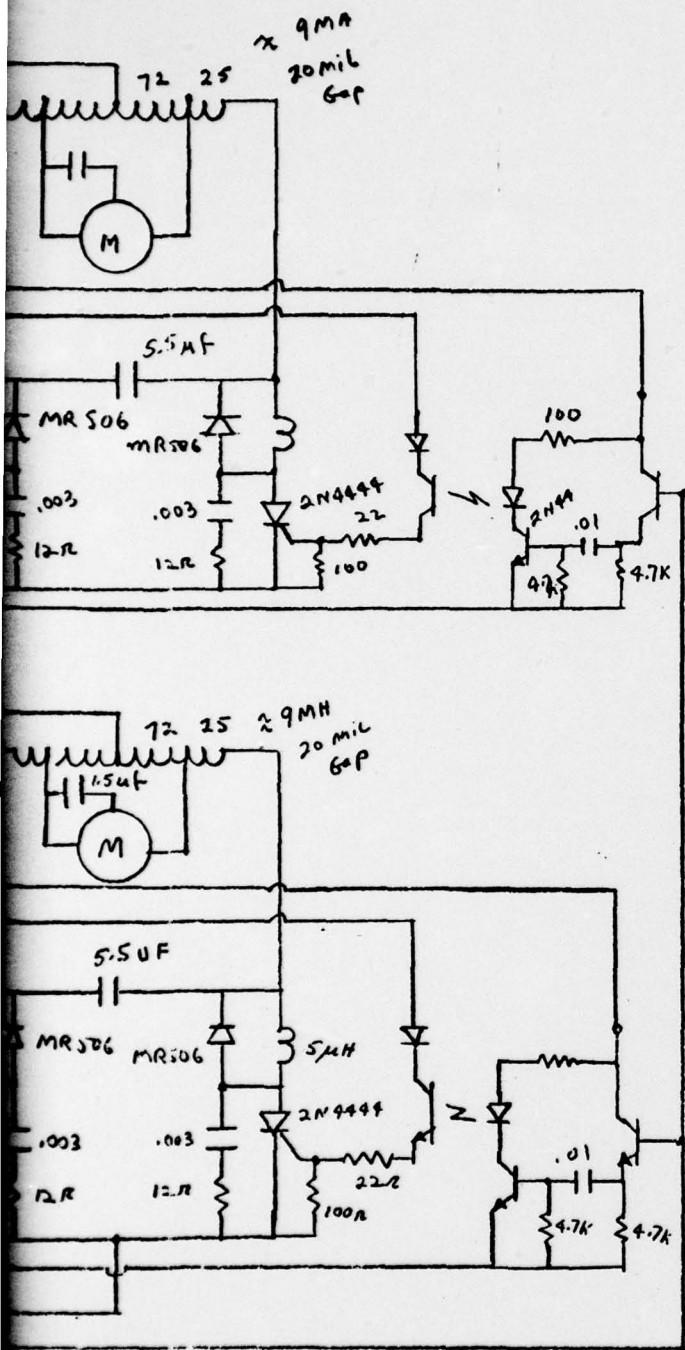


FIGURE 3.2.9-1

AUXI



AUXILIARY POWER SUPPLY

12 Aug 1976

The supply receives its input power as soon as the main power switch is turned on. Almost immediately the fan motor comes on. After an RC delay relay K₁ pulls in causing the main contactor to close. As long as this relay is closed power and frequency selection on the front panel is inhibited by an interlock on both switches.

The generated 400 Hz is a square wave caused by chopping the rectified power supply voltage. Rectification occurs via diodes D₂₀₀, D₂₀₁, D₂₀₂, D₂₀₃, D₂₀₄, D₂₀₅ and D₂₀₆. A split capacitor arrangement is used to reduce the voltage across each chopper to a reasonable value to allow for the use of small inexpensive SCR. Two circuits are used to improve reliability. Thus even if one circuit fails power is still supplied to the system.

3.2.10 MECHANICAL

Mechanically, the inverter is housed in a rectangular container. This container is constructed using aluminum for light weight without severe loss of mechanical strength.

A pictoral view showing the front panel configuration is shown in Figure 3.2.10-1. The system has a power on switch, a standby switch, and a power output switch. First the power on switch is switched on, next the standby switch is connected, and finally the output power switch is connected allowing a contactor to be pulled in to apply power to the inverter and to physically select the operating modes via another set of contactors. Once power comes on, both the frequency switch and the mode switch are disabled. Three connectors are required to provide the output power. When the 120 volt single phase output is selected and a suitable size connector is connected to the power output, the inverter is capable of producing 120 volts single phase 15 KW of power. When the 240 volt single phase output is selected, the inverter is capable of producing 240 volts single phase at 10 KW. When the three phase output is selected, the system is capable of generating three phase 120 volts, 5 KW per phase, with 4 wire output three phases plus neutral. For operation as a delta, the neutral is not used.

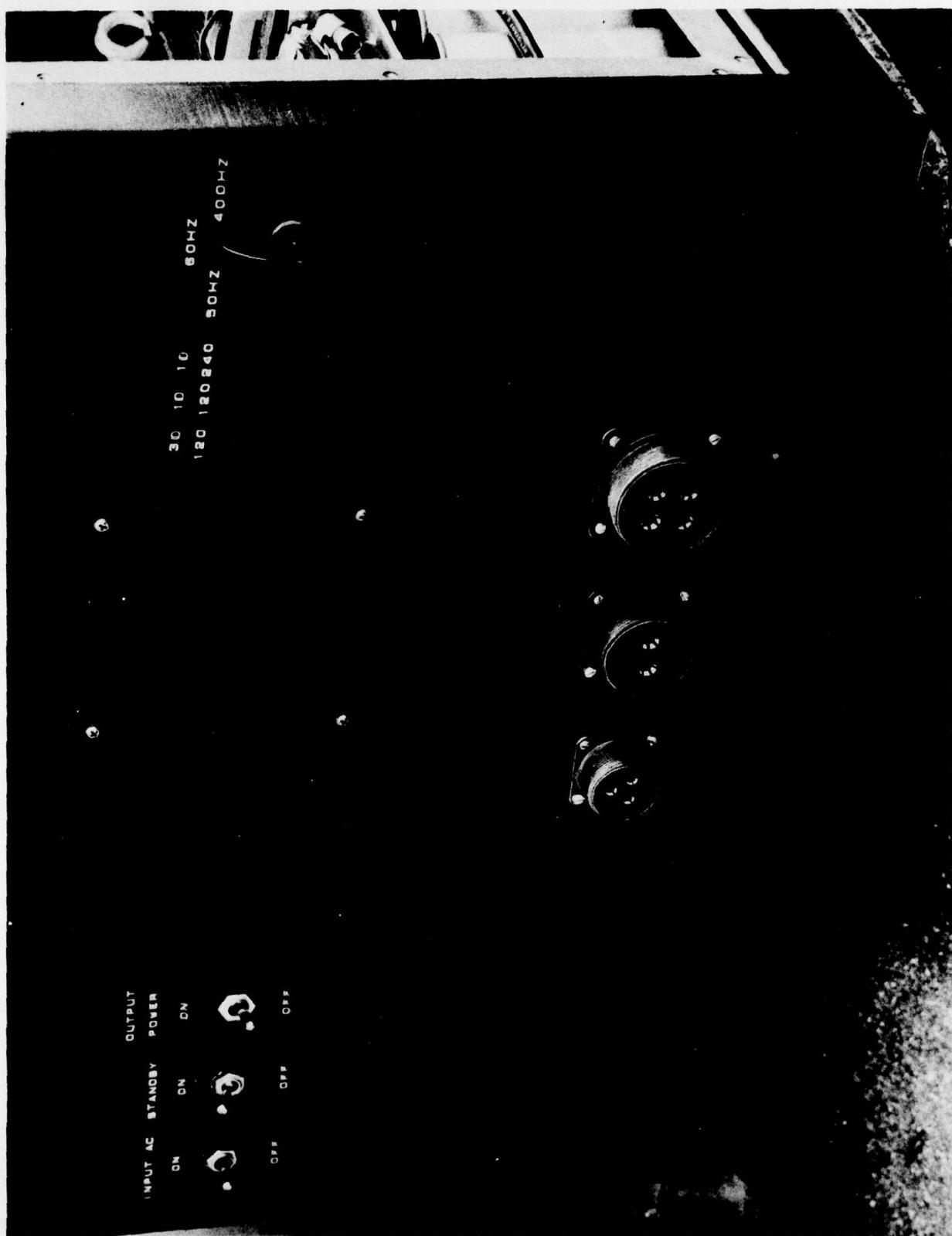


FIGURE 3.2.10-1 FRONT PANEL

Frequency selection is accomplished using the three position selector switch. The output of the switch is connected to the frequency select inputs on the buffer module.

Input power is connected through the rear panel of the inverter.

Air inlets are on the rear panel of the inverter. Exiting air is drawn out of the unit using two Rotron fans on the rear panel of the inverter.

4.0 CONCLUSIONS AND RECOMMENDATIONS

Based upon the data recorded and measurements made, the feasibility of a 15 KW inverter was established which is lighter in weight than those presently being used by about 200%, and it weighs about 50% of the nearest known competitive unit. Thus, it must be concluded that the use of the Texas Instrument 400 volt, 100 ampere integrated power switch IPS can provide significant savings over existing SCR designs.

It is also recommended that some improvements in the system be incorporated in future design. Some of these improvements include:

1. Use of permalloy powder cores in the output filter to further reduce weight and improve switching losses.
2. Incorporation of a controlled "power on" feature to provide easy on to the input power supply.
3. Reduction of power supply capacitor bank to further reduce system weight.
4. The incorporation of feedforward and feedback feature to reduce filter gain effects.
5. The incorporation of a variable carrier frequency which will further improve regulation and reduce harmonics.
6. The use of a higher speed processor such that the buffer memory can be eliminated and the transient responses can be further improved.
7. The utilization of aluminum bus bar wherever possible.

8. The incorporation of an auxiliary power supply comprising transistor technology instead of SCR.
9. The use of a simplified switch module for voltage boost instead of the SCR.
10. The incorporation of digital readout on the front panel for voltage monitoring.
11. The protection of the system against catastrophic failures which could potentially occur under adverse load conditions.
12. The incorporation of master/slave technology to allow for connecting together of more than one integrated power inverter in a manner which allows for paralleling inverter outputs to achieve higher wattage.
13. The incorporation of MPU control of short circuits on the switch to reduce present switch cost.
14. A complete computer analysis of the output filters to provide for output filter optimization.